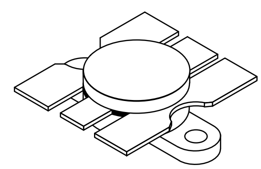
The RF Line
NPN Silicon RF Power Transistor

MRF644

25 W, 470 MHz
CONTROLLED Q
RF POWER
TRANSISTOR
NPN SILICON

. . . designed for 12.5 Volt UHF large–signal amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Specified 12.5 Volt, 470 MHz Characteristics —
  Output Power = 25 Watts
  Minimum Gain = 6.2 dB
  Efficiency = 60%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Built–In Matching Network for Broadband Operation
- Tested for Load Mismatch Stress at all Phase Angles with 20:1 VSWR @ 16–Volt High Line and 50% Overdrive
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



CASE 316–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	4.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	103 0.59	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	5.0	mAdc

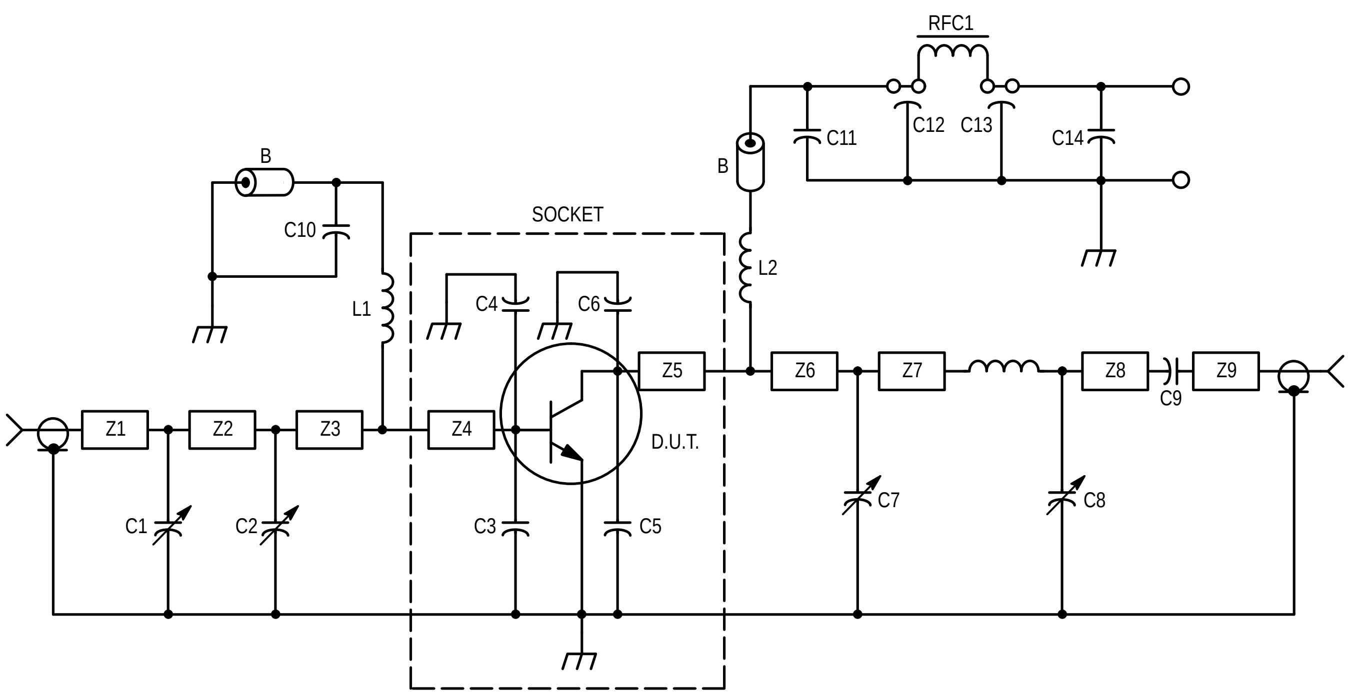
(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40	70	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	60	85	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 25 W, I_C (MAX) = 3.6 Adc, f = 470 MHz)	G_{pe}	6.2	7.0	—	dB
Input Power (V_{CC} = 12.5 Vdc, P_{out} = 25 W, f = 470 MHz)	P_{in}	—	5.0	6.0	Watts
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 25 W, I_C (MAX) = 3.6 Adc, f = 470 MHz)	η	55	60	—	%
Output Mismatch Stress (V_{CC} = 16 Vdc, P_{in} = Note 1, f = 470 MHz, VSWR = 20:1, All Phase Angles)	ψ *	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 25 W, f = 470 MHz)	Z_{in}	—	1.2 + j3.3	—	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 25 W, f = 470 MHz)	Z_{OL}	—	1.9 + j2.1	—	Ohms

NOTE:
1. P_{in} = 150% of Drive Requirement for 25 W Output at 12.5 Vdc.

* ψ = Mismatch stress factor — the electrical criterion established to verify the device resistance to load mismatch failure. The mismatch stress test is accomplished in the standard test fixture (Figure 1) terminated in a 20:1 minimum load mismatch at all phase angles.



C1, C2, C7, C8 — 1.0–20 pF Johanson Variable
C3 — 27 pF 100 mil ATC
C4 — 30 pF 100 mil ATC
C5, C6 — 33 pF 100 mil ATC
C9 — 250 pF 100 mil ATC
C10 — 100 pF UNELCO
C11, C14 — 1.0 µF 35 V TANTALUM
C12, C13 — 680 pF Feedthrough
L1 — 5″ #22 AWG 0.100″ ID
L2 — 5″ #20 AWG 0.187″ ID
RFC1 — Ferroxcube VK200–20–4B
B — Ferroxcube Bead 56–590–65–3B
Z1 — 0.25″ x 0.20″ Microstrip
Z2 — 1.63″ x 0.20″ Microstrip
Z3 — 0.20″ x 0.20″ Microstrip
Z4, Z5 — 1/2″ #18 AWG bent in a "V" shape 1/8″ Wide
Z6 — 0.20″ x 0.20″ Microstrip
Z7 — 0.70″ x 0.20″ Microstrip
Z8 — 0.33″ x 0.20″ Microstrip
Z9 — 0.50″ x 0.20″ Microstrip
Board — 62.5 mil Glass Teflon, ϵ_r = 2.55

Figure 1. Test Circuit Schematic

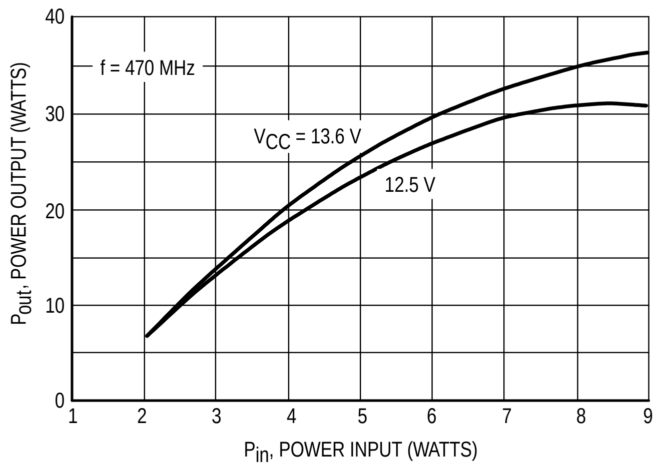


Figure 2. Power Output versus Power Input

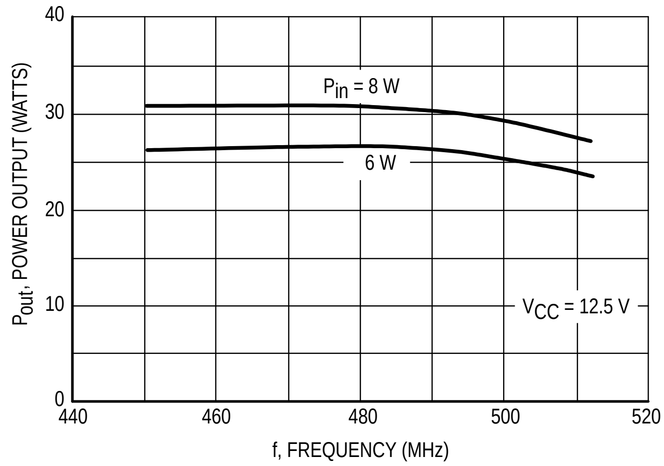


Figure 3. Power Output versus Frequency

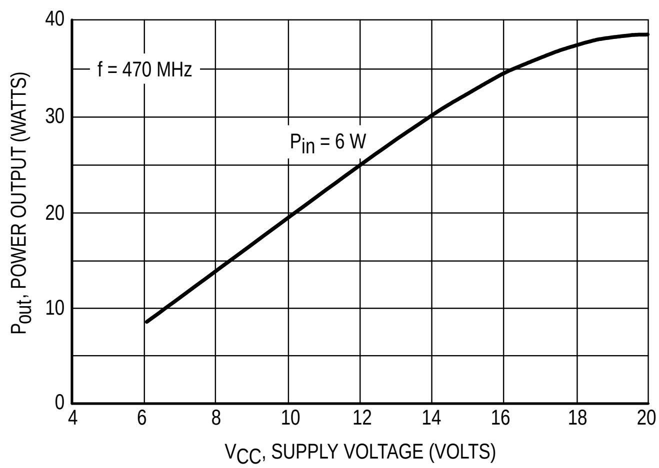


Figure 4. Power Output versus Supply Voltage

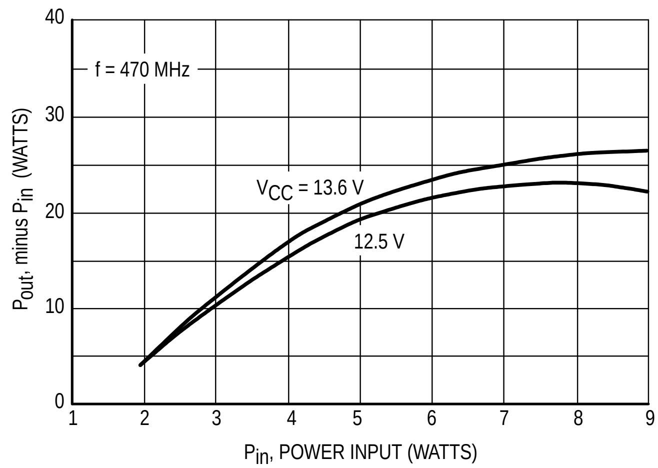
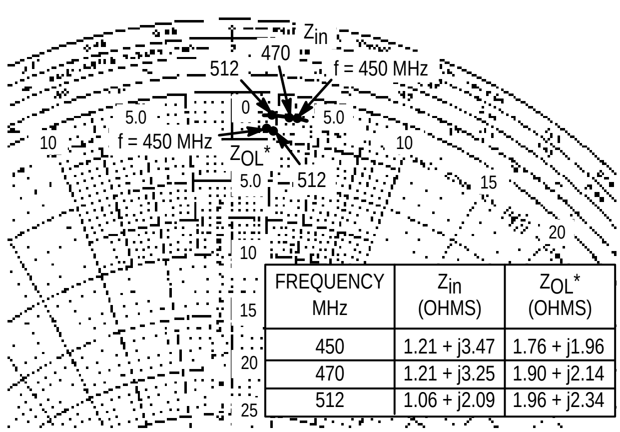


Figure 5. Power Saturation Profile

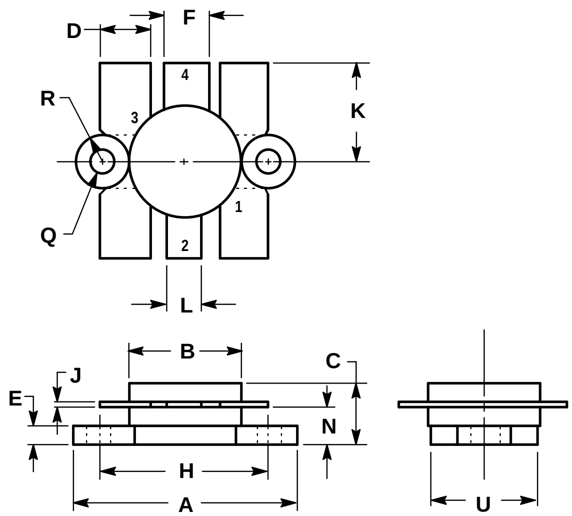


FREQUENCY MHz	Z_{in} (OHMS)	Z_{OL}* (OHMS)
450	1.21 + j3.47	1.76 + j1.96
470	1.21 + j3.25	1.90 + j2.14
512	1.06 + j2.09	1.96 + j2.34

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 6. Series Equivalent Input–Output Impedance

PACKAGE DIMENSIONS



NOTES:
1. FLANGE IS ISOLATED IN ALL STYLES.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	24.38	25.14	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.58	0.210	0.220
E	2.16	3.04	0.085	0.120
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	11.17	0.405	0.440
L	3.81	4.06	0.150	0.160
N	3.81	4.31	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130
U	11.94	12.57	0.470	0.495

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE

CASE 316–01
ISSUE D

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