The RF Line

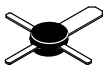
NPN Silicon RF Low Power Transistor

MRF555

Designed primarily for wideband large signal predriver stages in the UHF frequency range.

- Specified @ 12.5 V, 470 MHz Characteristics @ P_{out} = 1.5 W
  Common Emitter Power Gain = 12.5 dB (Typ)
  Efficiency 60% (Typ)
- Cost Effective PowerMacro Package
- Electroless Tin Plated Leads for Improved Solderability
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

1.5 W, 470 MHz
RF LOW POWER
TRANSISTOR
NPN SILICON



CASE 317D–02, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	400	mAdc
Operating Junction Temperature	T_J	150	°C
Total Device Dissipation @ T_C = 75°C (1, 2) Derate above 75°C	P_D	3.0 40	Watts mW/°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

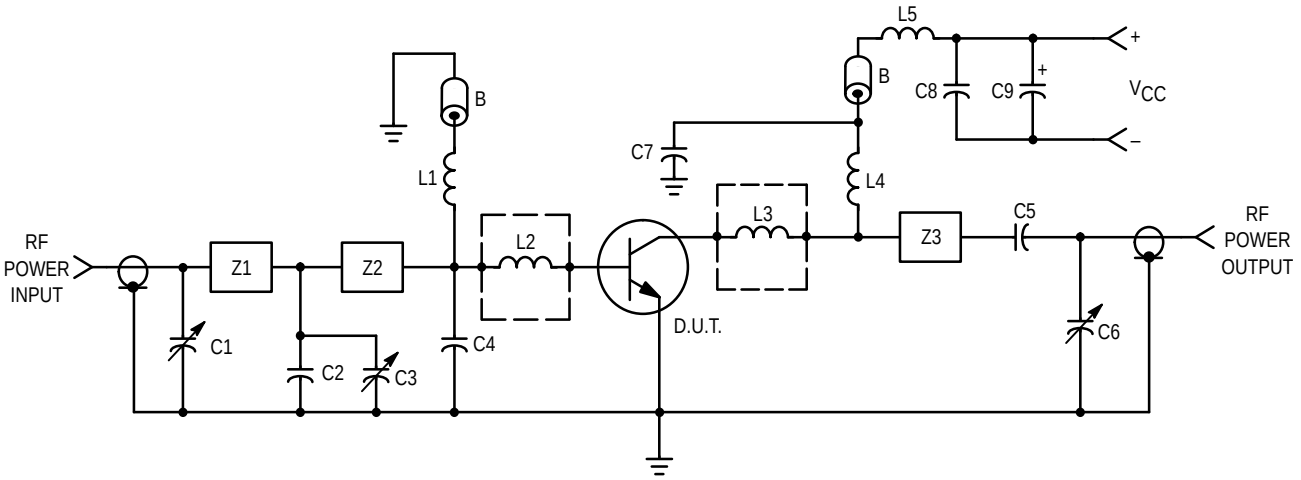
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	50	90	200	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	3.5	5.0	pF

NOTES: (continued)

1. T_C, Case temperature measured on collector lead immediately adjacent to body of package.
2. The MRF555 PowerMacro must be properly mounted for reliable operation. AN938, “Mounting Techniques in PowerMacro Transistor,” discusses methods of mounting and heatsinking.

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (f = 470 MHz)					
Common–Emitter Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W)	G_{pe}	11	12.5	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W)	η_c	50	60	—	%
Load Mismatch Stress (V_{CC} = 15.5 Vdc, P_{in} = 125 mW, VSWR ≥ 10:1 all phase angles)	ψ	No Degradation in Output Power			



*C1, C3, C6 — 0.8–11 pF Johanson
C2 — 15 pF Clamped Mica, Mini–Underwood
C4 — 36 pF Clamped Mica, Mini–Underwood
C5 — 470 pF Ceramic Chip Capacitor
C7 — 91 pF Clamped Mica, Mini–Underwood
C8 — 68 pF Clamped Mica, Mini–Underwood
C9 — 1.0 μF, 25 V Tantalum
B — Bead, Ferroxcube 56–590–65/3B

*Fixed tuned for broadband response

L1 — 5 Turns #21 AWG, 5/32″ I.D.
L2, L3 — 60 x 125 x 250 Mils Copper Pad on 27 Mil Thick Alumina Substrate
L4, L5 — 7 Turns #21 AWG 5/32″ I.D.
Z1 — 1.29″ x 0.16″ Microstrip
Z2 — 0.70″ x 0.16″ Microstrip
Z3 — 2.18″ x 0.16″ Microstrip

PCB — 1/16″ Glass Teflon, 1 oz. cu. clad, double sided, ε_r = 2.5

Figure 1. 400–512 MHz Broadband Circuit

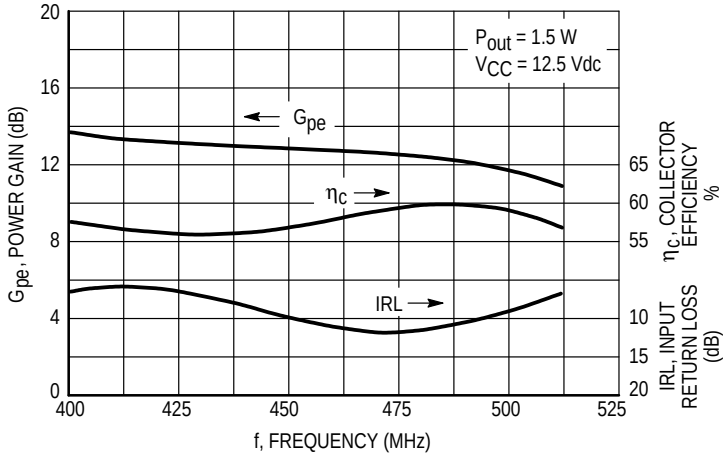


Figure 2. Performance in Broadband Circuit

f Frequency MHz	Z_{in} Ohms		Z_{OL}* Ohms	
	V_{CC} = 7.5 V	V_{CC} = 12.5 V	V_{CC} = 7.5 V	V_{CC} = 12.5 V
	P_{in} = 100 mW	P_{in} = 50 mW	P_{out} 400 MHz = 1.5 W P_{out} 450 MHz = 1.35 W P_{out} 512 MHz = 1.05 W	P_{out} 400 MHz = 1.9 W P_{out} 450 MHz = 1.45 W P_{out} 512 MHz = 0.9 W
400	2.9 – j2.7	1.9 – j3.1	18.0 – j13.4	12.2 – j19.7
450	2.2 – j0.8	2.6 – j4.0	21.6 = j9.9	20.2 – j18.6
512	3.5 – j1.2	2.6 – j2.6	20.1 – j1.0	23.4 – j23.0

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Table 1. Z_{in} and Z_{OL} versus Collector Voltage, Input Power and Output Power

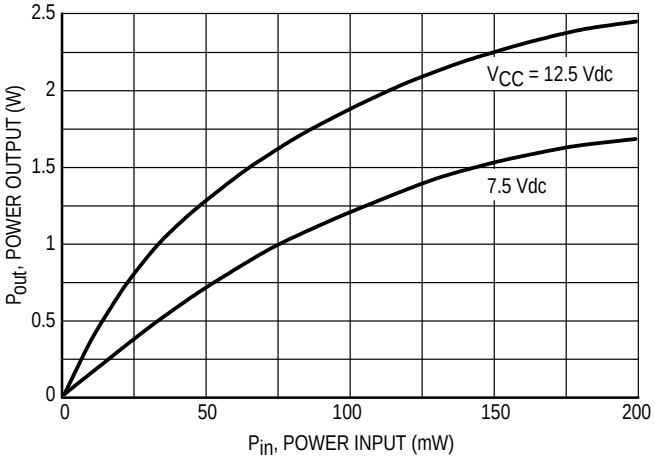


Figure 3. Power Output versus Power Input

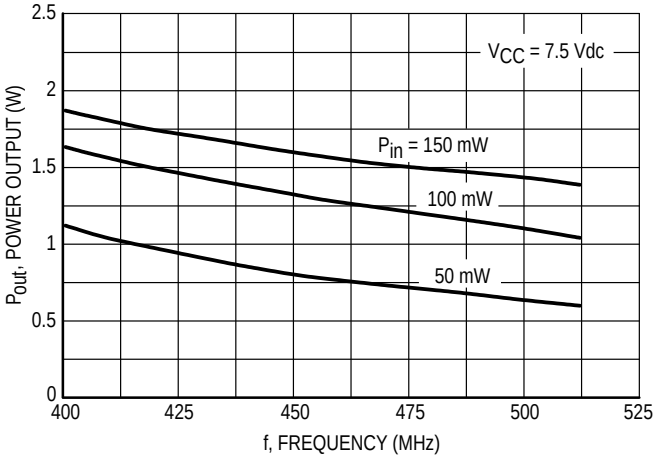


Figure 4. Power Output versus Frequency

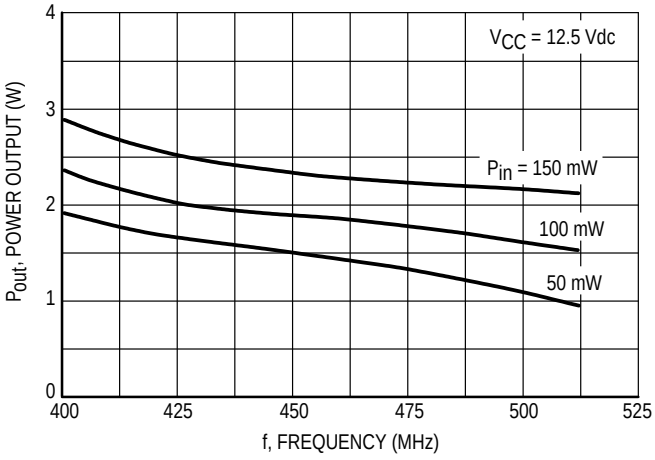


Figure 5. Power Output versus Frequency

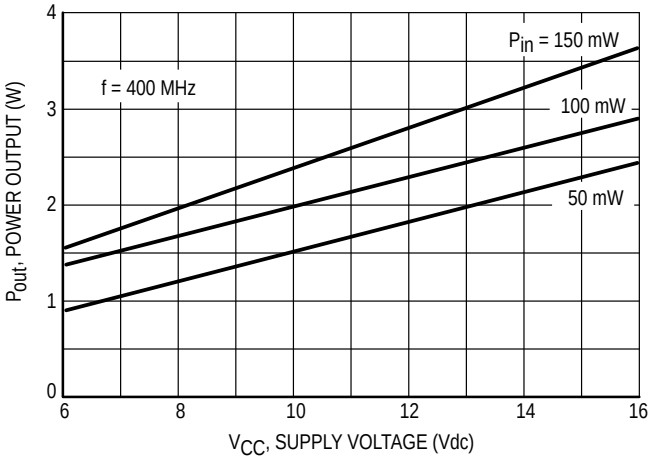


Figure 6. Power Output versus Supply Voltage

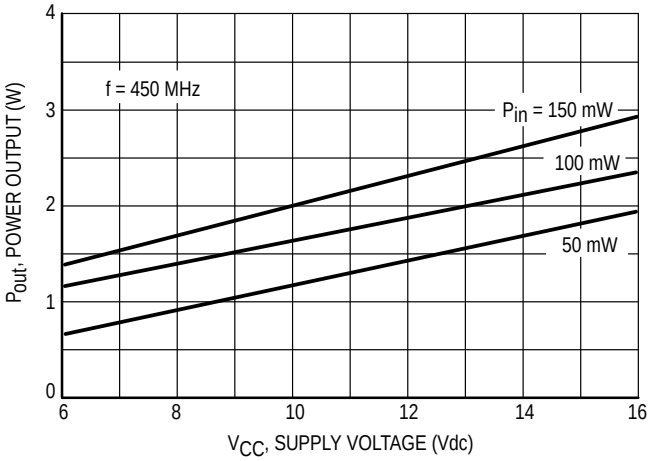


Figure 7. Power Output versus Supply Voltage

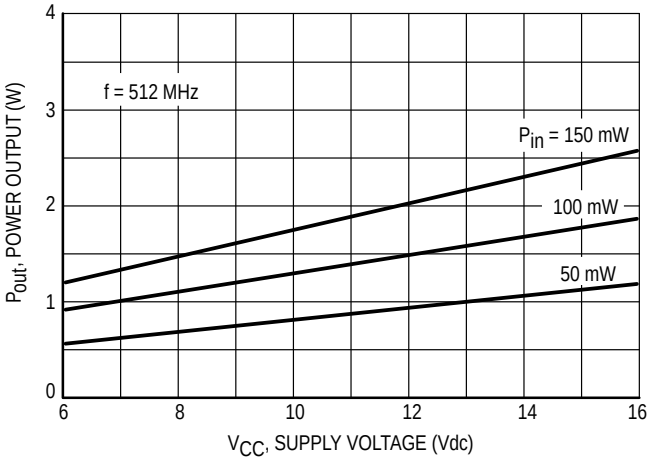
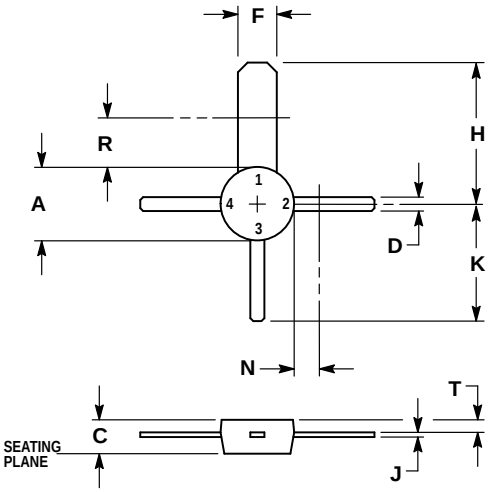


Figure 8. Power Output versus Supply Voltage

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. LEAD DIMENSIONS UNCONTROLLED WITHIN DIMENSION N AND R.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
C	0.075	0.100	1.91	2.54
D	0.033	0.039	0.84	0.99
F	0.097	0.104	2.46	2.64
H	0.348	0.383	8.84	9.72
J	0.008	0.012	0.24	0.30
K	0.285	0.320	7.24	8.12
N	—	0.065	—	1.65
R	—	0.128	—	3.25
T	0.025	0.040	0.64	1.01

STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

CASE 317D–02
ISSUE C

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