

Silicon Controlled Rectifiers

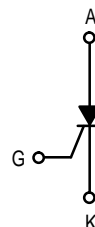
Reverse Blocking Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

- Small Size
- Passivated Die for Reliability and Uniformity
- Low Level Triggering and Holding Characteristics
- Available in Two Package Styles
 - Surface Mount Lead Form — Case 369A
 - Miniature Plastic Package — Straight Leads — Case 369

ORDERING INFORMATION

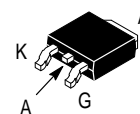
- To Obtain "DPAK" in Surface Mount Leadform (Case 369A)
 - Shipped in Sleeves — No Suffix, i.e. MCR8DSN
 - Shipped in 16 mm Tape and Reel — Add "T4" Suffix to Device Number, i.e. MCR8DSNT4
- To Obtain "DPAK" in Straight Lead Version (Case 369) Shipped in Sleeves — Add "-1" Suffix to Device Number, i.e. MCR8DSN-1



MCR8DSM
MCR8DSN

Motorola Preferred Devices

SCRs
8.0 AMPERES RMS
600 thru 800 VOLTS



CASE 369A-13
STYLE 4

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (1) Peak Repetitive Reverse Voltage ($T_J = -40$ to 110°C , $R_{GK} = 1.0\text{ K}\Omega$)	V_{DRM} V_{RRM}	600 800	Volts
On-State RMS Current (All Conduction Angles; $T_C = 90^\circ\text{C}$)	$I_T(\text{RMS})$	8.0	Amps
Average On-State Current (All Conduction Angles; $T_C = 90^\circ\text{C}$)	$I_T(\text{AV})$	5.1	
Peak Non-Repetitive Surge Current (One Half Cycle, 60 Hz, $T_J = 110^\circ\text{C}$)	I_{TSM}	90	
Circuit Fusing Consideration ($t = 8.3\text{ msec}$)	I^2t	34	A^2sec
Peak Gate Power (Pulse Width $\leq 10\ \mu\text{sec}$, $T_C = 90^\circ\text{C}$)	P_{GM}	5.0	Watts
Average Gate Power ($t = 8.3\text{ msec}$, $T_C = 90^\circ\text{C}$)	$P_{G(\text{AV})}$	0.5	
Peak Gate Current (Pulse Width $\leq 10\ \mu\text{sec}$, $T_C = 90^\circ\text{C}$)	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	-40 to 110	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40 to 150	

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	2.2	$^\circ\text{C}/\text{W}$
— Junction to Ambient	$R_{\theta JA}$	88	
— Junction to Ambient (2)	$R_{\theta JA}$	80	
Maximum Lead Temperature for Soldering Purposes (3)	T_L	260	$^\circ\text{C}$

(1) V_{DRM} for all types can be applied on a continuous basis. Ratings apply for negative gate voltage or $R_{GK} = 1.0\text{ K}\Omega$; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.

(2) Surface mounted on minimum recommended pad size.

(3) 1/8" from case for 10 seconds.

Preferred devices are Motorola recommended choices for future use and best overall value.

MCR8DSM MCR8DSN

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$; $R_{GK} = 1.0\text{ K}\Omega$ unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Peak Reverse Gate Blocking Voltage ($I_{GR} = 10\ \mu\text{A}$)	V_{GRM}	10	12.5	18	Volts
Peak Forward Blocking Current Peak Reverse Blocking Current ($V_{AK} = \text{Rated } V_{DRM} \text{ or } V_{RRM}$) (1) $T_J = 25^\circ\text{C}$ $T_J = 110^\circ\text{C}$	I_{DRM} I_{RRM}	— —	— —	10 500	μA
Peak Reverse Gate Blocking Current ($V_{GR} = 10\ \text{V}$)	I_{RGM}	—	—	1.2	μA
Peak On-State Voltage (2) ($I_{TM} = 16\ \text{A}$)	V_{TM}	—	1.4	1.8	Volts
Gate Trigger Current (Continuous dc) (3) ($V_D = 12\ \text{V}$, $R_L = 100\ \Omega$, $T_J = 25^\circ\text{C}$) ($V_D = 12\ \text{V}$, $R_L = 100\ \Omega$, $T_J = -40^\circ\text{C}$)	I_{GT}	5.0 —	12 —	200 300	μA
Gate Trigger Voltage (Continuous dc) ($V_D = 12\ \text{V}$, $R_L = 100\ \Omega$, $T_J = 25^\circ\text{C}$) ($V_D = 12\ \text{V}$, $R_L = 100\ \Omega$, $T_J = -40^\circ\text{C}$) ($V_D = 12\ \text{V}$, $R_L = 100\ \Omega$, $T_J = 110^\circ\text{C}$)	V_{GT}	0.45 — 0.2	0.65 — —	1.0 1.5 —	Volts
Holding Current ($V_D = 12\ \text{V}$, $I_{\text{init}} = 200\ \text{mA}$, $T_J = 25^\circ\text{C}$) ($V_D = 12\ \text{V}$, $I_{\text{init}} = 200\ \text{mA}$, $T_J = -40^\circ\text{C}$)	I_H	0.5 —	1.0 —	6.0 10	mA
Latching Current ($V_D = 12\ \text{V}$, $I_G = 2.0\ \text{mA}$, $T_J = 25^\circ\text{C}$) ($V_D = 12\ \text{V}$, $I_G = 2.0\ \text{mA}$, $T_J = -40^\circ\text{C}$)	I_L	0.5 —	1.0 —	6.0 10	mA

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Total Turn-On Time (Source Voltage = $12\ \text{V}$, $R_S = 6.0\ \text{K}\Omega$, $I_T = 16\ \text{A(pk)}$, $R_{GK} = 1.0\ \text{K}\Omega$) ($V_D = \text{Rated } V_{DRM}$, Rise Time = $20\ \text{ns}$, Pulse Width = $10\ \mu\text{s}$)	tgt	—	2.0	5.0	μs
Critical Rate of Rise of Off-State Voltage ($V_D = 0.67 \times \text{Rated } V_{DRM}$, Exponential Waveform, $R_{GK} = 1.0\ \text{K}\Omega$, $T_J = 110^\circ\text{C}$)	dv/dt	2.0	10	—	$\text{V}/\mu\text{s}$

(1) Ratings apply for negative gate voltage or $R_{GK} = 1.0\ \text{K}\Omega$. Devices shall not have a positive gate voltage concurrently with a negative voltage on the anode. Devices should not be tested with a constant current source for forward and reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

(2) Pulse Test; Pulse Width $\leq 2.0\ \text{msec}$, Duty Cycle $\leq 2\%$.

(3) Does not include R_{GK} current.

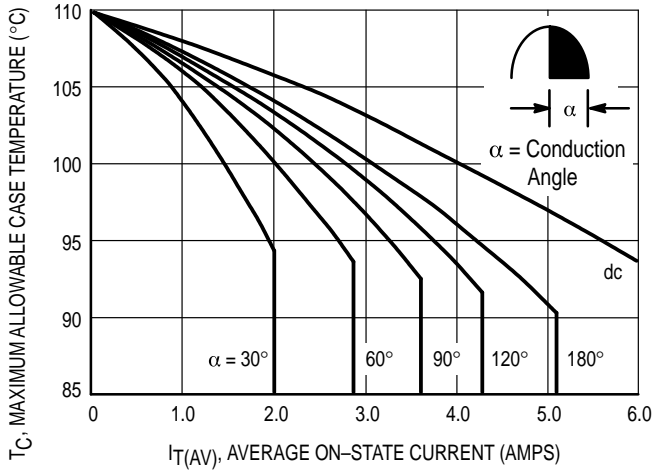


Figure 1. Average Current Derating

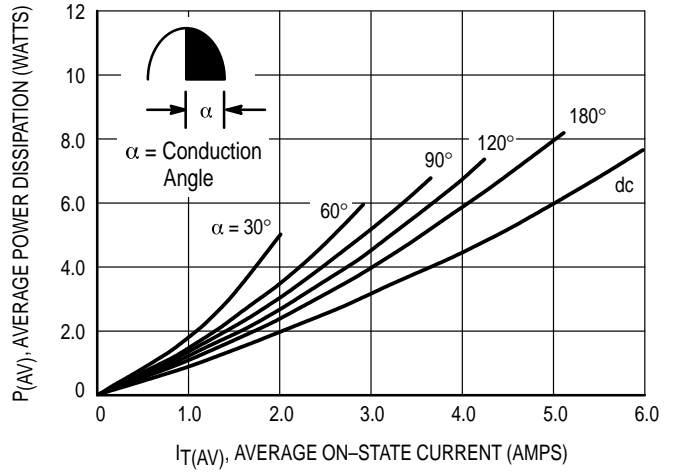


Figure 2. On-State Power Dissipation

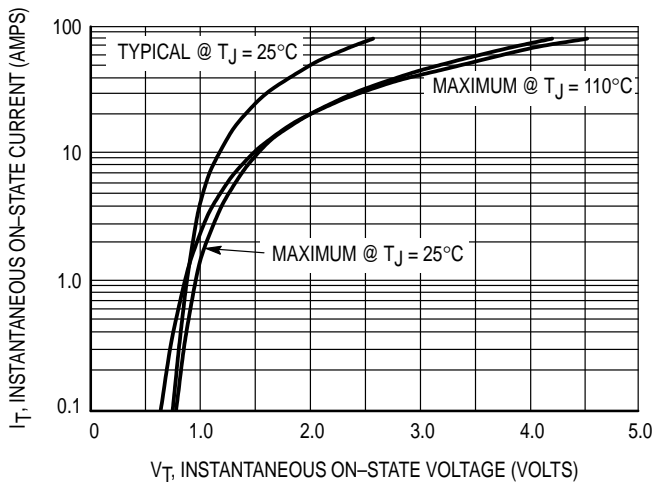


Figure 3. On-State Characteristics

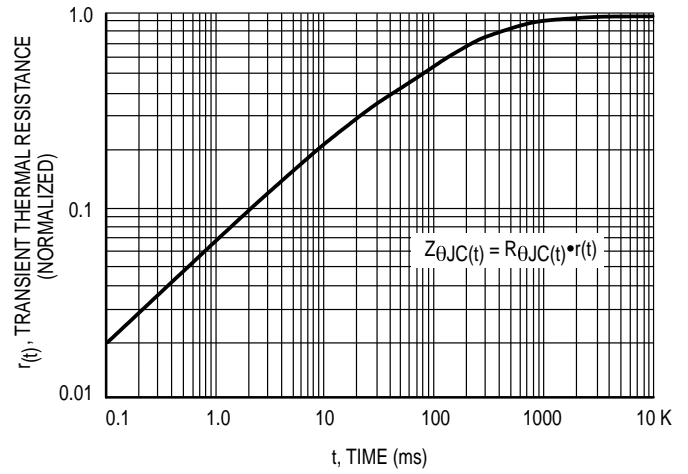


Figure 4. Transient Thermal Response

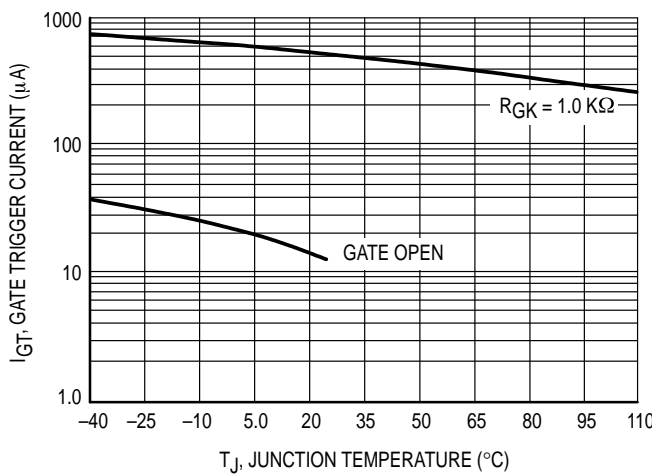


Figure 5. Typical Gate Trigger Current versus Junction Temperature

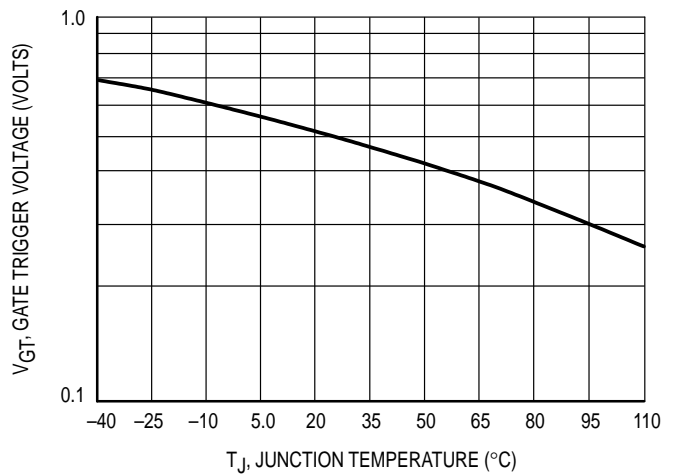


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

MCR8DSM MCR8DSN

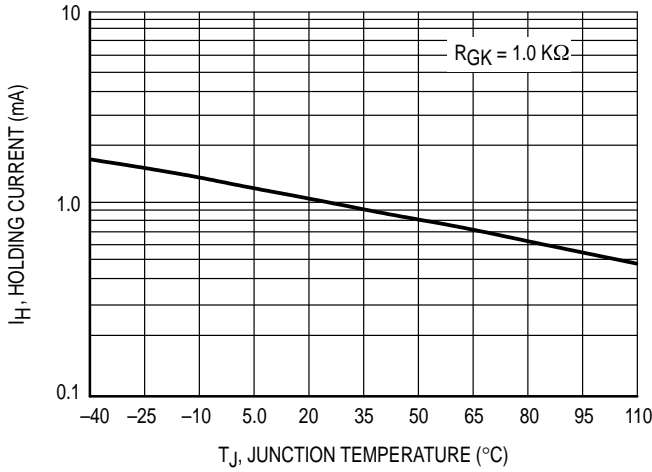


Figure 7. Typical Holding Current versus Junction Temperature

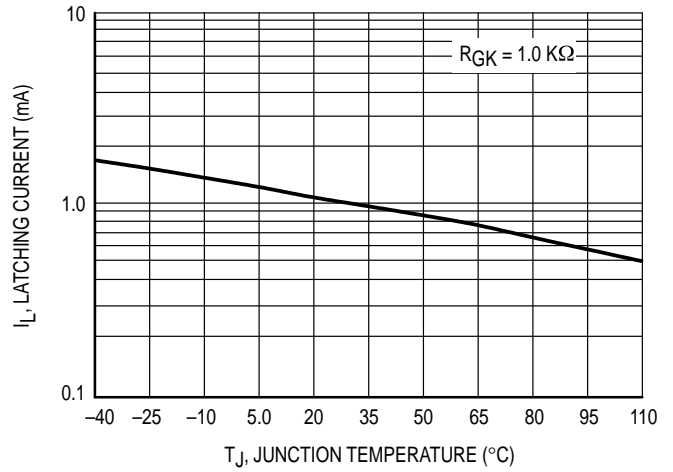


Figure 8. Typical Latching Current versus Junction Temperature

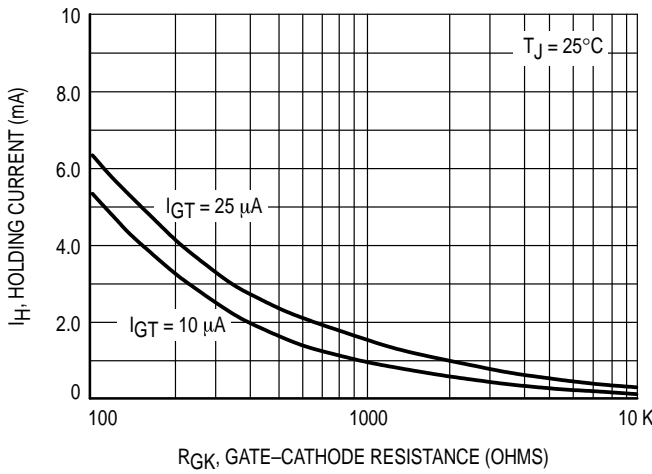


Figure 9. Holding Current versus Gate-Cathode Resistance

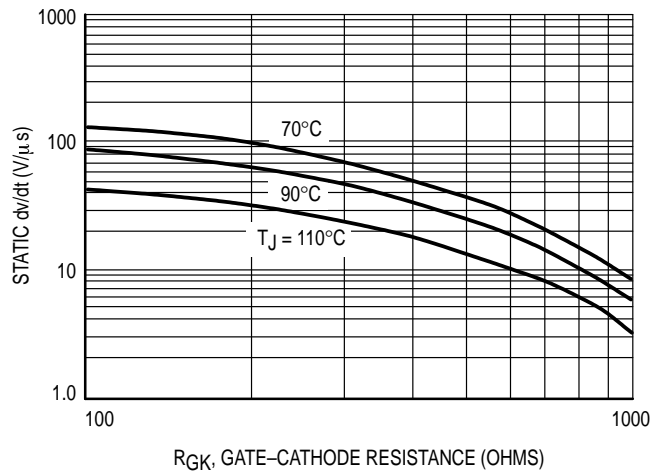


Figure 10. Exponential Static dv/dt versus Gate-Cathode Resistance and Junction Temperature

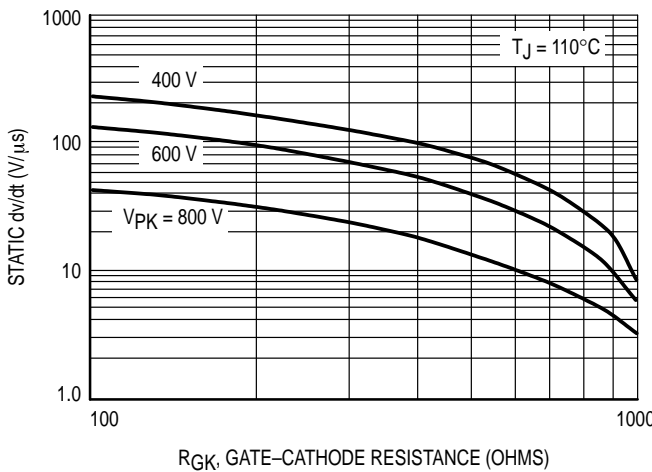


Figure 11. Exponential Static dv/dt versus Gate-Cathode Resistance and Peak Voltage

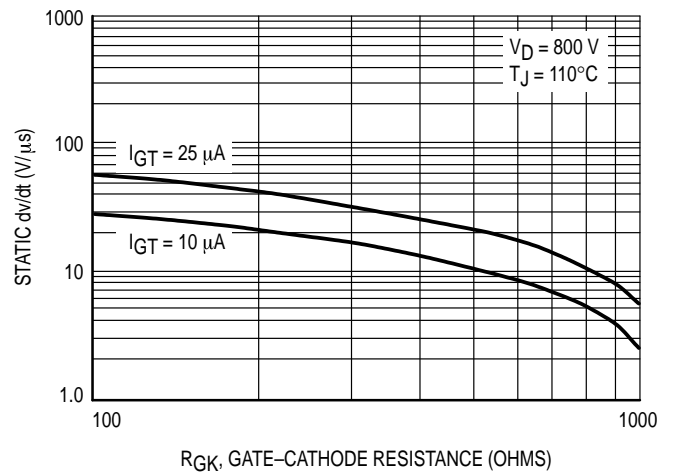
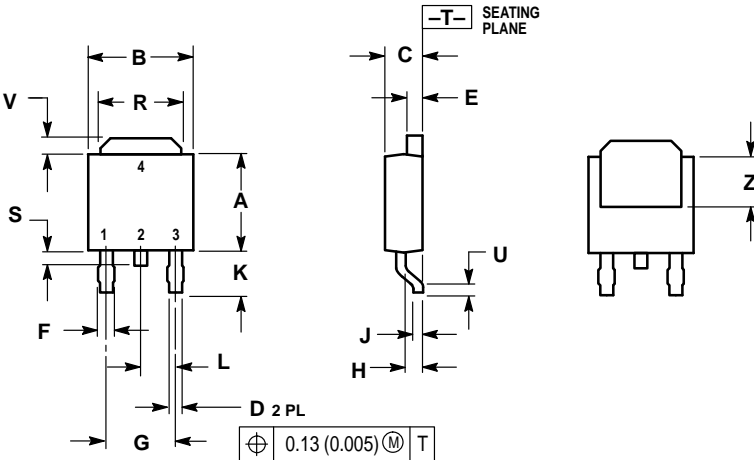


Figure 12. Exponential Static dv/dt versus Gate-Cathode Resistance and Gate Trigger Current Sensitivity

PACKAGE DIMENSIONS



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	—	0.51	—
V	0.030	0.050	0.77	1.27
Z	0.138	—	3.51	—

STYLE 4:
 PIN 1. CATHODE
 2. ANODE
 3. GATE
 4. ANODE

CASE 369A-13
 ISSUE Y

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How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303-675-2140 or 1-800-441-2447

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 4-32-1,
Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan. 81-3-5487-8488

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
– US & Canada ONLY 1-800-774-1848

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

INTERNET: <http://motorola.com/sps>

