Quality and Reliability Assurance

The ability to build and maintain the high levels of quality and reliability today, depends on inherent design and process capability, and not the degree of test and inspection. Both the design and production facilities for Power MOSFETs are totally new, with state-of-the-art equipment and process techniques which deliver this needed capability.

In-Process Quality Control

All critical phases of the highly automated power MOSFET manufacturing cycle have been characterized with respect to their intrinsic variability. Statistical limits have been established to give warning of abnormal process trends and fluctuations, based on this intrinsic capability. These limits are constantly tightened as the process improves and are well within the engineering specifications. The emphasis at Harris is to employ statistical methods at the point of control, rather than an inspection point at the end of a process.

Control of Outgoing Product

The quality control lot acceptance sampling of finished product is performed after manufacturing has performed 100% inspection of all specified electrical characteristics. The current sampling level is 0.1% AQL for electrical parameters, and is constantly being improved. However, due to tight parameter distributions gained through process control and inherent design capability, the average outgoing quality level (AOQ) to the customer has been in the order of 100 PPM (0.01%).

Reliability Assurance

Harris Semiconductor has a world-wide reliability program that helps to shape the direction of new product development, assures that the reliability level is maintained throughout the production cycle, and develops specific models to predict the reliability in the end-use application. In order to meet these objectives, a reliability facility is maintained at each manufacturing location for real-time feedback. A centralized reliability engineering organization develops all new test methods and supports new product/process development. Each group is fully trained in the reliability and applied statistics disciplines, as well as failure analysis, and are responsible for using these techniques to monitor and improve product capability.

The Reliability Program

The reliability-assurance program operates at all stages of production, using the following four-pronged approach:

Product Design and Development

During early development, initial product lots are characterized through accelerated reliability tests which establish the product capability. Once the design had been fine-tuned, multiple production runs are initiated and samples are subjected to a full range of standardized accelerated tests. All lots must meet pre-established reliability standards before any new design or process can be released for production.

Wafer HTRB

Harris Semiconductor has developed a totally unique in-line reliability test performed at the wafer level. Samples from each wafer lot receive a 24-hour +150^{o}C bias life test to measure passivation integrity and surface cleanliness.

Real Time Indicators (RTI)

RTI's are short-duration accelerated-stress tests used to control the occurrence of specific failure mechanisms that can significantly affect product reliability. The stress levels are designed to induce failures, so that product-capability shifts can be detected and corrected. They are performed weekly at each manufacturing location. In this real-time method of determining reliability, a continuous flow of data is provided to indicate how well the manufacturing process is performing product.

TABLE 1. TYPICAL MOSFET RTI TESTS

TEST	CONDITIONS	PACKAGE	TYPICAL DURATION
Power Cycling	PD = 4.75W T_J = +35^{o}C - 175^{o}C (approx.)	Plastic	10 - 15K Cycles
Power Cycling	PD = 4.75W T_J = +35^{o}C - 175^{o}C (approx.)	TO-3	20 - 50K Cycles
D-S Bias Life	T_A = +150^{o}C 80% of Drain Source	All	168 Hours
G-S Bias Life	G - S = 16V T_A = +150^{o}C	All	168 Hours

Requalification Program (RQP)

Each product is requalified every six to twelve months to the same matrix of tests required for the initial production release. This operation measures the changes in the total capability of each MOSFET family to meet the original reliability design objectives. Table 2 is typical of the data generated for RQP.

TABLE 2. ACCELERATED POWER MOSFET TEST RELIABILITY SUMMARY

PACKAGE	TEST AND CONDITIONS	DURATION	CUM. HOURS OR CYCLES	% NON-FUNCTIONAL
All	Bias Life Drain-Source = 80% of rated T_A = +150°C	500 Hours	300,000	0.33
All	Bias Life Gate-Source = 16V, T_A = +150°C	500 Hours	270,000	0.00
All	Operating Life T_A = +150°C, Free Air	500 Hours	230,000	0.00
TO-31 TO-39	Thermal Cycling -65°C to +150°C	400 Cycles	133,600	0.30
TO-220	Thermal Shock -65°C to +150°C	400 Cycles	100,000	0.00
TO-31 TO-39	Power Cycling Delta T_J = +78°C PD = 56W (TO-3) or 2W (TO-39)	20,000 Cycles	5,480K	0.73
TO-220	Power Cycling Delta T_J = +135°C, PD = 4.75W	10,000 Cycles	1,850K	0.00
TO-220	Pressure Cooker	24 Hours	3,072	0.00

FAILURE RATE IN %/1000 HOURS AT 60% UCL			
TEST	**T_A = +125°C**	**T_A = +90°C**	**T_A = +75°C**
Bias Life	0.09	0.005	0.001
Operating Life	0.07	0.004	0.001

NOTE: Failure rate based on Nonfunctional performance in an operating mode, extrapolated from +150°C data using 1.0eV activation energy.