An6870

DOT MATRIX LCD CONTROLLER & DRIVER

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FUNCTION

- Character type dot matrix LCD controller and driver
- Easy Interface with a 4-bit or 8-bit microprocessors
- Wide range of various instruction functions
- Standard and extended operation modes for applications flexibility
- Mask programming of extended functions in standard/extended modes according to the Order Form
- Mask programming of the desired customer's characters table
- 1 line of 5x8 or 5x11 dot or 2 lines of 5x8 dot characters display
- Advanced controller version An6870A with the Large Font mode: 10x15 dot character format and Icon line
- Chip and Mode Identifier allows to detect chip version and current state of controller
- Internal driver: 16 common and 80 segment signal outputs
- Interface with the An6865 or An6863 extension driver to increase number of displayed characters (up to 80)
- Build-in automatic power-on reset function
- Internal oscillator with one external resistor

FEATURES

- Power Supply Voltage: 2.7V to 5.5V
- LCD Driving Voltage: 3.0V to 11V
- Two types of Display Waveforms:
  - A-type (line inversion)
  - B-type (frame inversion)
- High-speed MPU bus interface - 2 MHz (at 5V Power Supply)
- Display Data RAM size is 80 x 8 bits for 80 characters
- Character Generator ROM size is 20480 bits with two pages:
  - 2 pages with 240 characters of 5x8 dot format for each or
  - 1 page with 240 5x11 dot characters or
  - combination of 2 pages region with 5x8 dot characters and 1 page region with 5x11 dot characters or
  - 126 characters of 10x15 dot format for Large Font mode
- Character Generator RAM size is 64 x 8 bits for:
  - 8 characters of 5x8 dot format or
  - 4 characters of 5x11 dot format or
  - 2 characters of 10x15 dot format or 20x15 bitmap for Large Font mode
- Programmable duty cycle:
  - 1/8 duty for one line of 5x8 dot characters
  - 1/11 duty for one line of 5x11 dot characters
  - 1/16 duty for two lines of 5x8 dot characters and Large Font mode
- Low power consumption

Ordering Information

Version	Description
An6870-xxyy	Controller version with full function set for Standard and Extended modes
An6870S-xxyy	Controller version only for Standard mode (XMODE=1 or NC)
An6870A-xxyy	Controller version for Large Font mode

Note: xx – Functional mask option number,
yy – CGROM pattern number

An6870 Versions Comparision

Parameter	An6870 (Standard mode)	An6870 (Extended mode)	An6870A (Large Font mode)
Character format	5x8 or 5x11	5x8 or 5x11	up to 10x15 (Text-type LCD) up to 8x15 (Graphics-type LCD)
Maximum number of characters, displayed with internal SEG outputs	16 (1 line) 32 (2 lines)	16 (1 line) 32 (2 lines)	8 (1 line) + 32 icons
Maximum number of displayed characters with extension driver	80 (1 line) 2x40 (2 lines)	80 (1 line) 2x40 (2 lines)	40 (1 line) + 160 icons
Number of character codes stored in DDRAM	80	80	40 characters + 160 icons
Number of characters in CGROM	240[1)]	up to 2x248[2)]	126
Number of characters stored in CGRAM	8 characters 5x8 or 4 characters 5x11	8 characters 5x8 or 4 characters 5x11	2 characters
COM/SEG outputs	16/80	16/80	16/80
Duty cycle	1/8, 1/11 or 1/16	1/8, 1/11 or 1/16	1/16
Type of LCD	Text	Text	Text or Graphics
LCD drive waveform	A-type or B-type[3)]	A-type or B-type[3)]	A-type or B-type[3)]
Oscillator:			
• clock source	External frequency or external resistor	External frequency or external resistor	External frequency or external resistor
• clock frequency	270kHz±30%	270kHz±30%	400 kHz ±30%
• frame frequency	- 83 Hz (1/8 or 1/16 duty) - 61.5 Hz (for 1/11 duty)	- 83 Hz (1/8 or 1/16 duty) - 61.5 Hz (for 1/11 duty)	- 60 Hz (1/16 duty)
• external resistor	91KΩ±2% (for V_{DD}=5V) 75KΩ±2% (for V_{DD}=3V)	91KΩ±2% (for V_{DD}=5V) 75KΩ±2% (for V_{DD}=3V)	62 KΩ±2% (for V_{DD}=5V) 56 KΩ±2% (for V_{DD}=3V)
Maximum MPU bus frequency	2MHz	2MHz	2MHz
Instruction execution time (except Display Clear)	31.5 μs (8.5 cycles at Fosc=270kHz)	31.5 μs (8.5 cycles at Fosc=270kHz)	21.25 μs (8.5 cycles at Fosc=400kHz)
Instructions set	fully compatible with analogues	compatible with analogues, additional functions	Mainly compatible with analogues, additional functions
Additional functions[4)]:			
• 2-page CGROM	(-)	(+)	-
• Large Font mode	-	-	+
• Chip Identifier	+	+	+
• Advanced 4-bit interface	+	+	+
• Cursor blink	(-)	(+)	+
• Display inversion enable	(-)	(+)	(+)

Notes:

1) There is arbitrary relationship between number of 5x8 dot and 5x11 dot characters available. Number of CGROM characters may be increased up to 248.
2) There is a second page for 5x8 dot characters available. 5x11 dot characters are the same for the first and the second pages. Enable of second page selection, CGROM characters pattern and address range for second page are selected by the Customer in the Order Form.
3) Display Waveform type for LCD is selectable by the Customer in the Order Form.
4) Characters (-) and (+) mean that functions in this operation mode may be changed (enabled or disabled respectively) by the Customer when filling in the Order Form.

INTRODUCTION

The An6870 is a dot matrix LCD controller designed for display of alphanumeric data. It has standard compatible mode and extended mode with larger CGROM size and additional service functions.

The An6870 has 16 COM and 80 SEG outputs to display one 5x8 or 5x11 dot character line, or two 5x8 dot character lines. With internal segment outputs the controller can display up to 16 characters in each line (up to 32 characters in two-line mode). Extension drivers increase number of displayed characters to 80 (up to 40 characters in a line for two-line mode).

The displayed character codes are written into the 80-byte Display Data RAM (DDRAM). Character patterns are stored in the 20,480-bit Character Generator ROM (CGROM) or 64x8-bit Character Generator RAM (CGRAM). The CGROM capacity allows to code two pages of 5x8 dot characters or one 5x11 dot character page (up to 248 characters on each page). Mixed format coding is also allowed. In the CGRAM the user can write eight 5x8 dot characters or four 5x11 dot characters.

The An6870A version is designed to display large size characters of 10x15 dot format. In this case it is possible to display 8 characters using the controller's own segment drivers or up to 40 characters in a line with the extension drivers. Simultaneously 160 icons can be displayed, 4 icons per each displayed character. The CGROM can contain up to 126 large characters, and 2 large characters can be written into the CGRAM.

Data exchange with an external control device is performed by an easy-to-use system interface compatible with many MPU types. Also the controller has a wide instruction set. Instructions and data can be transferred via 4- or 8-bit data bus. The An6870 features an advanced 4-bit interface that allows synchronization of the internal controller state with the interface timing diagram.

The An6870 has a standard extension driver interface with An6865, An6863 and similar type drivers. COM and SEG waveforms can be "A" or "B" type. The type is selected in the Order Form.

Reset function initializes the controller automatically after power on.

The An6870 has a Chip and Mode IDentifier (CMID), that allows the external MPU to detect chip version, ROM code and service functions status, as well as the current operation mode, and to adjust the system operating according to received data.

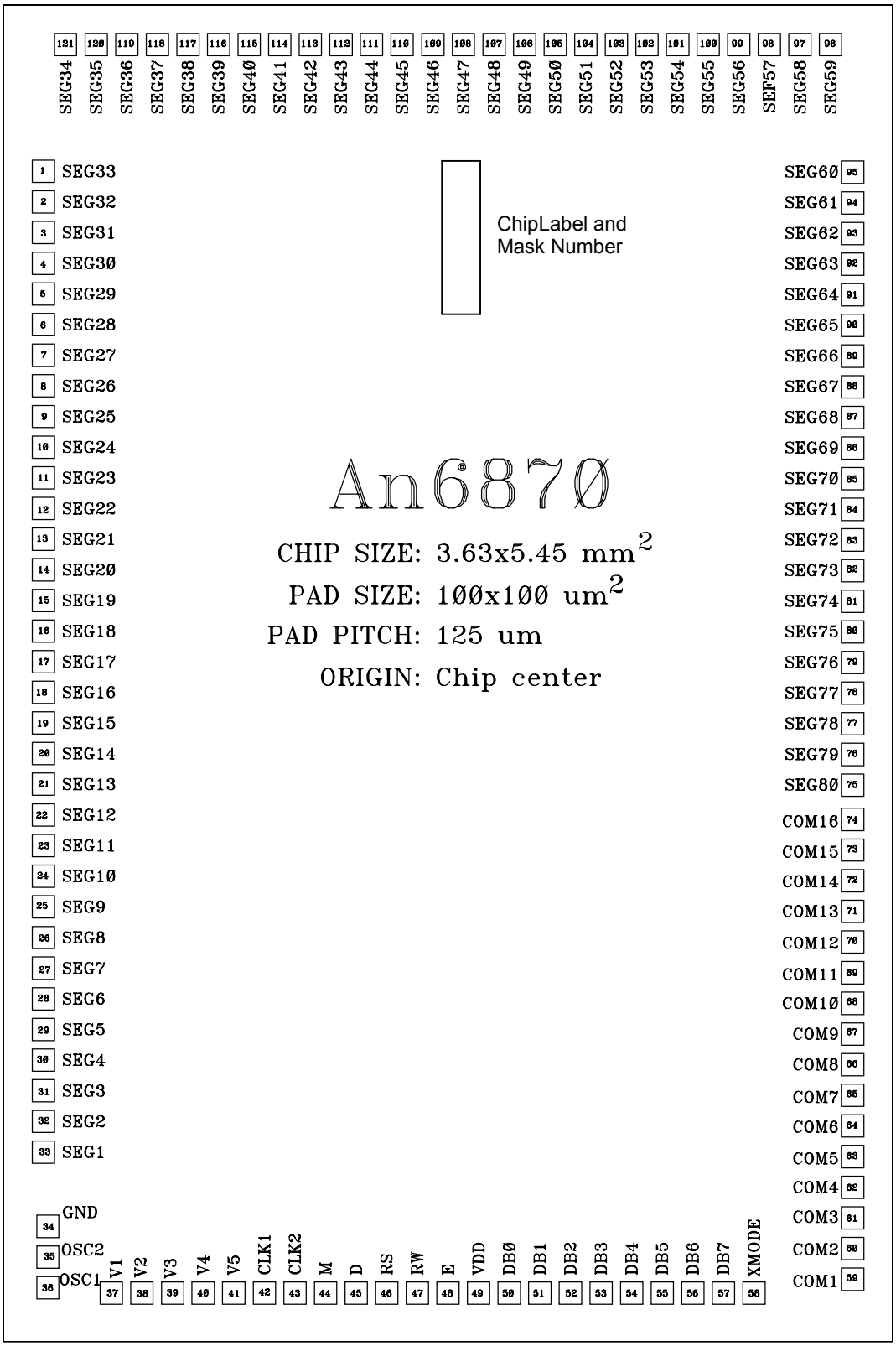
The controller is fabricated by the production single-metal CMOS technology. Mask programming of the CGROM, as well as initialization state, and the extended functions selection, are implemented by metal mask.

Therefore, the An6870 features three base operation modes*):

1) **The Standard compatible mode with basic function set. This mode is enabled when the XMODE pin is either not connected or set to the logic "1" state.**
2) **The Extended mode, allows to use extended functions. This mode is enabled when the XMODE pin is connected to GND or set to the logic "0" state. The extended functions include the use of two CGROM pages for 5x8 dot characters, the Display Inversion control capability, the cursor blinking mode (similar to the PC text mode cursor).**
3) **The Large Font mode, which is implemented in the An6870A version. It is programmed by mask option. This mode allows to display characters of larger size and with better quality (for this purpose a special CGROM mask option is required) as well as the Icons line. In this mode data can be output to the graphic LCD panel of the 16x80 and larger format because the character size makes it possible to leave spaces between adjacent characters.**

***) Note: Standard and Extended functions as well as CGROM character coding and the initial state after power on can be selected by the Customer when filling in the Order Form. Some functions can be made accessible in the Standard mode, others in the Extended mode. Certain functions can be accessible in both modes or disabled (see Order Form).**

PAD DIAGRAM


121 SEG34
120 SEG35
119 SEG36
118 SEG37
117 SEG38
116 SEG39
115 SEG40
114 SEG41
113 SEG42
112 SEG43
111 SEG44
110 SEG45
109 SEG46
108 SEG47
107 SEG48
106 SEG49
105 SEG50
104 SEG51
103 SEG52
102 SEG53
101 SEG54
100 SEG55
99 SEG56
98 SEF57
97 SEG58
96 SEG59
1 SEG33
2 SEG32
3 SEG31
4 SEG30
5 SEG29
6 SEG28
7 SEG27
8 SEG26
9 SEG25
10 SEG24
11 SEG23
12 SEG22
13 SEG21
14 SEG20
15 SEG19
16 SEG18
17 SEG17
18 SEG16
19 SEG15
20 SEG14
21 SEG13
22 SEG12
23 SEG11
24 SEG10
25 SEG9
26 SEG8
27 SEG7
28 SEG6
29 SEG5
30 SEG4
31 SEG3
32 SEG2
33 SEG1
ChipLabel and
Mask Number
SEG60 95
SEG61 94
SEG62 93
SEG63 92
SEG64 91
SEG65 90
SEG66 89
SEG67 88
SEG68 87
SEG69 86
SEG70 85
SEG71 84
SEG72 83
SEG73 82
SEG74 81
SEG75 80
SEG76 79
SEG77 78
SEG78 77
SEG79 76
SEG80 75
COM16 74
COM15 73
COM14 72
COM13 71
COM12 70
COM11 69
COM10 68
COM9 67
COM8 66
COM7 65
COM6 64
COM5 63
COM4 62
COM3 61
COM2 60
COM1 59
An6870
CHIP SIZE: 3.63x5.45 mm2
PAD SIZE: 100x100 um2
PAD PITCH: 125 um
ORIGIN: Chip center
34 GND
35 OSC2
36 OSC1
37 V1
38 V2
39 V3
40 V4
41 V5
42 CLK1
43 CLK2
44 M
45 D
46 RS
47 RW
48 E
49 VDD
50 DB0
51 DB1
52 DB2
53 DB3
54 DB4
55 DB5
56 DB6
57 DB7
58 XMODE

PAD LOCATION COORDINATES

Pad No	Pad Name	Coordinates		Pad No	Pad Name	Coordinates	
		X (μm)	Y (μm)			X (μm)	Y (μm)
1	SEG33	-1652.7	2047.3	62	COM4	1652.5	-2096.1
2	SEG32		1922.3	63	COM5		-1971.1
3	SEG31		1797.3	64	COM6		-1846.1
4	SEG30		1672.3	65	COM7		-1721.1
5	SEG29		1547.3	66	COM8		-1596.1
6	SEG28		1422.3	67	COM9		-1471.1
7	SEG27		1297.3	68	COM10		-1346.1
8	SEG26		1172.3	69	COM11		-1221.1
9	SEG25		1047.3	70	COM12		-1096.1
10	SEG24		922.3	71	COM13		-971.1
11	SEG23		797.3	72	COM14		-846.1
12	SEG22		672.3	73	COM15		-721.1
13	SEG21		547.3	74	COM16		-596.1
14	SEG20		422.3	75	SEG80		-456.3
15	SEG19		297.3	76	SEG79		-331.3
16	SEG18		172.3	77	SEG78		-206.3
17	SEG17		47.3	78	SEG77		-81.3
18	SEG16		-77.7	79	SEG76		43.7
19	SEG15		-202.7	80	SEG75		168.7
20	SEG14		-327.7	81	SEG74		293.7
21	SEG13		-452.7	82	SEG73		418.7
22	SEG12		-577.7	83	SEG72		543.7
23	SEG11		-702.7	84	SEG71		668.7
24	SEG10		-827.7	85	SEG70		793.7
25	SEG9		-952.7	86	SEG69		918.7
26	SEG8		-1077.7	87	SEG68		1043.7
27	SEG7		-1202.7	88	SEG67		1168.7
28	SEG6		-1327.7	89	SEG66		1293.7
29	SEG5		-1452.7	90	SEG65		1418.7
30	SEG4		-1577.7	91	SEG64		1543.7
31	SEG3		-1702.7	92	SEG63		1668.7
32	SEG2		-1827.7	93	SEG62		1793.7
33	SEG1		-1952.7	94	SEG61		1918.7
34	GND	-1635.1	-2255.9	95	SEG60		2043.7
35	OSC2		-2380.9	96	SEG59	1562.4	2563.6
36	OSC1		-2505.9	97	SEG58	1437.4	
37	V1	-1375.5	-2527.5	98	SEG57	1312.4	
38	V2	-1250.5		99	SEG56	1187.4	
39	V3	-1125.5		100	SEG55	1062.4	
40	V4	-1000.5		101	SEG54	937.4	
41	V5	-875.5		102	SEG53	812.4	
42	CLK1	-750.5		103	SEG52	687.4	
43	CLK2	-625.5		104	SEG51	562.4	
44	M	-500.5		105	SEG50	437.4	
45	D	-375.5		106	SEG49	312.4	
46	RS	-250.5		107	SEG48	187.4	
47	RW	-125.5		108	SEG47	62.4	
48	E	-0.5		109	SEG46	-62.6	
49	VDD	124.4		110	SEG45	-187.6	
50	DB0	249.5		111	SEG44	-312.6	
51	DB1	374.5		112	SEG43	-437.6	
52	DB2	499.5		113	SEG42	-562.6	
53	DB3	624.5		114	SEG41	-687.6	
54	DB4	749.5		115	SEG40	-812.6	
55	DB5	874.5		116	SEG39	-937.6	
56	DB6	999.5		117	SEG38	-1062.6	
57	DB7	1124.5		118	SEG37	-1187.6	
58	XMODE	1249.5		119	SEG36	-1312.6	
59	COM1	1652.5	-2471.1	120	SEG35	-1437.6	
60	COM2		-2346.1	121	SEG34	-1562.6	
61	COM3		-2221.1				

PIN DESCRIPTION

Pin Name	Lines	Input/output	Description	Interface
V_{DD}	1	-	Positive voltage for logical circuit and LCD drivers	Power supply
GND	1	-	Ground (0V)	Power supply
V1 - V5	5	-	Bias voltage level for LCD driving from Power supply or resistive divider: $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$. V_5 – negative bias voltage: V_{DD}-V_5=V_{LCD}.	Power supply
COM1 - COM16	16	output	Common signal outputs for LCD driving	LCD
SEG1 - SEG80	80	output	Segment signal outputs for LCD driving	
OSC1, OSC2	2	input OSC1 output OSC2	When using internal oscillator, connect external resistor. If external clock is used, connect it to OSC1 (OSC2 open).	external resistor or external oscillator
CLK1	1	output	Extension driver latch clock	Extension driver
CLK2	1	output	Extension driver shift clock	
M	1	output	The alternating signal to change polarity of LCD driver voltage.	
D	1	output	Output extension driver data.	
RS	1	input (pull-up to V_{DD})	Used as Interface register selection input. When RS=1 Data register is selected. When RS=0 Instruction register is selected (when writing) or Busy flag state and current address (when reading).	MPU
RW	1	input (pull-up to V_{DD})	Used as read/write selection input. When RW=1 - reading operation When RW=0 – writing operation.	
E	1	input	Used as read/write enable signal.	
DB0 - DB3	4	input / output (pull-up to V_{DD})	Used as low order bi-directional data bus, when 8 bit bus mode. Not used, when 4-bit bus mode.	
DB4 - DB7	4	input / output (pull-up to V_{DD})	Used as high order bi-directional data bus, when 8-bit bus mode. Used as both high and low order, when 4-bit bus mode pins are. DB7 used for Busy flag output.	
XMODE	1	input (pull-up to V_{DD})	Used as operation mode switch signal: XMODE=1 – standard mode, XMODE=0 – extended mode.	MPU or control circuit

FUNCTIONAL DESCRIPTION OF AN6870

1. OVERVIEW

The An6870 internally provides all necessary functions to display characters. The chip including interface with MPU, DDRAM, CGRAM and CGROM, LCD drivers and extended drivers interface to increase number of displaying characters. This controller allows to build information displaying systems with minimum of external components. It is possible to display one line with 5x8 or 5x11 characters or two lines with 5x8 characters.

Block Diagram is shown in Figure 1.

The An6870 is controlled by instructions from MPU interface. The interface contains 8-bit data bus DB[7..0], interface operation enable pin (E), read/write mode pin (RW), data register or instructions register select pin (RS).

The controller can interface with MPU by two ways:

- by using 8-bit data bus and 3 control signals (totally 11 interface lines);
- by using 4 high-order bits of data bus (totally 7 interface lines), thus 4-bit data transferred twice (with two E pulses). For increase reliability of data transferring special synchronization mechanism for 4-bit groups is used.

The controller is operated through 2 input buffer registers: IR (Instruction Register) and DR (Data Register). Instructions and data are written into the selected register with E fall, then interface is locked out for the instruction execution time. Instructions are executed according to internal timing diagram independently of interface functioning. Busy Flag (BF) is used to check the state of current instruction execution. Before sending the next instruction to the controller, MPU must check BF and make sure that previous instruction is finished and input registers are open for new data and instructions.

This interface model allows to operate with high-frequency bus independently from slow internal timing diagram of the controller, which forms internal cycles of instruction executing, memory access and display waveform.

Each instruction execution is accompanied with data reading from internal memory into output Data Register (DR). MPU can read this data by next Data Read instruction.

The controller has 4 classes of instructions:

- designate controller functions (Function Set, Entry Mode Set, Display Clear, Display on/off, Cursor on/off, Blinking on/off);
- set internal RAM addresses (Set DDRAM/CGRAM Address, Return Home);
- perform data transfer with internal memory;
- perform miscellaneous functions.

The controller contains 3 memory units:

- DDRAM: contains codes of displayed characters (80 bytes). Character order in DDRAM corresponds to character order on LCD;
- CGROM: contains font table. CGROM contains up to 240 (248) characters at code range 16 (8) to 255. Coding of 5x8 or 5x11 dot characters is available, 5x8 dot characters may be allocated in two pages.
- CGRAM with 64-byte capacity for user characters (totally 8 characters 5x8 dots or 4 characters 5x11 dots). CGRAM occupies 16 (8) character codes from 0 to 15 (7). If CGRAM or its part is not used for user characters, it may be used as general purpose RAM.

Chip and Mode Identifier (CMID) allows external device to read type, chip version and current state of controller. CMID allows to increase system functionality and reliability.

Controller memory (DDRAM or CGRAM) is allocated according to current address stored in Address Counter (AC). It means that before random access to memory, it is necessary to write Set CGRAM/DDRAM Address instruction. After execution of any read/write instruction, AC address automatically changes by 1. Direction of AC address change depends on "ID" control bit of Entry Mode Set instruction.

Address Counter also defines cursor position on LCD.

The controller also has mode in which data write combines with display shift. It means that character code writing into DDRAM, address auto increment, and display backward shift take place simultaneously. Visually the cursor is stable and the character line is shifting. This mode is enabled by "S" control bit of "Entry mode Set" instruction.

Autoincrement feature allows to simplify controller programming for end-user applications.

DDRAM addressing depends on display format. In 1-line mode, single address range from 0 to 79 for all 80 characters is used. In 2-line mode, DDRAM address is divided into two ranges: from 0 to 39 for the first line and from 64 to 103 for the second line. When sequential incrementing or decrementing of AC address counter, DDRAM address passes both ranges, accordingly the cursor moves from the first line to the second and vice versa.

Character code read from DDRAM during display refresh time is used to select its pattern from the CGROM or CGRAM. Data from Character Generator is transformed to sequential form and written into SEG shift register at each CLK2 strobe. When SEG shift register if filled with data for next COM (display row), data is transferred from shift register to SEG outputs latches at CLK1 strobe synchronously with switching to the next COM, and data appears in all driver outputs and on the LCD.

The controller has 80 SEG (display column) drivers for displaying first 16 characters per line. To increase number of displayed characters, it is possible to use extension drivers such as An6865 (40 SEG) or An6863 (80 SEG). Extension drivers are connected to the controller through driver interface, which contains 4 outputs:

- CLK2 – data shift strobe,
- CLK1 – data latch strobe,
- D – serial data output for shift register extension,
- M – alternating signal for polarity change of LCD voltage.

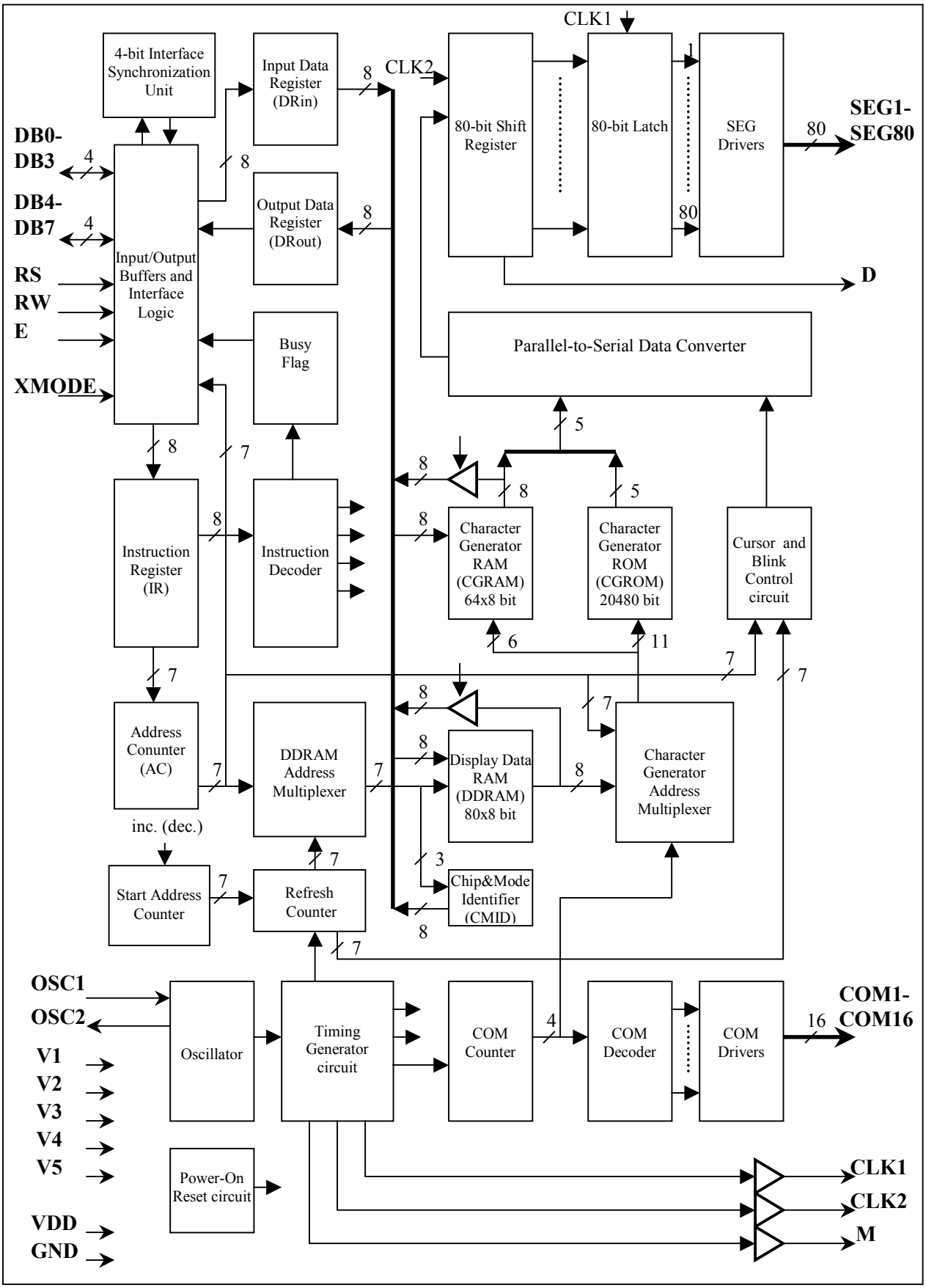


Figure 1. An6870 Block Diagram.

Functional diagram can be divided into the following parts:

1) **Logic control circuit:**
   - MPU bus interface,
   - Instruction decoder,
   - Address Counter (AC),
   - Start Address Counter,
   - Oscillator and Timing generator,
   - Timers for COM cycle and character/cursor blinking,
   - Cursor forming circuit,
   - Power-on Reset circuit.
2) **Memory circuit:**
   - Display Data RAM (DDRAM),
   - Character Generator RAM (CGRAM),
   - Character Generator ROM (CGROM),
   - Chip and Mode Identifier (CMID),
   - Memory access control circuits, address and data multiplexer.
3) **LCD drivers circuit with voltage level shift:**
   - Parallel-to-serial data converter for transfer Character Generator data to SEG shift register,
   - COM counter & decoder,
   - COM drivers,
   - SEG shift register and output latches,
   - SEG drivers,
   - Extension drivers interface.

2. LOGIC CONTROL CIRCUIT

2.1. MPU bus interface

Interface registers

The An6870 has two 8-bit interface registers: instruction register (IR) and data register (DR). Instruction register is write-only and it stores instruction codes. Data register is read/write (write – DRin, read – DRout). Data exchange between registers and MPU perform through bi-directional Data Bus (DB).

Registers are selected by RS signal, and read/write operations are selected by RW signal (refer to table 1).

Table 1 Interface Register selection

RS	RW	Operation
0	0	Writing instructions into IR
0	1	Reading Busy Flag (DB7) and Address Counter (DB6-DB0)
1	0	Writing data into DR
1	1	Reading data from DR

The IR register is used to store instruction code while instruction executing.

The DR register is used for temporary storage of data to be read/write to DDRAM or CGRAM. While executing any instruction RAM data always is read automatically, thus DRout always contains data from the last address (even if the address was changed during instruction execution). This data can be read from DB-bus by the next read instruction. It is guaranteed that MPU always receives data from the last address.

The main function of interface registers is separating MPU interface timing diagram from internal controller timing diagram. The IR and DR registers allow to release MPU data bus during instruction execution. While instruction execution, registers are locked, and information in registers can't be changed.

Busy Flag (BF)

Before writing the next instruction, MPU must ensure that previous instruction is completed and interface registers are free. To make this, MPU can check Busy Flag (BF). If BF=1, the controller is executing the previous instruction, and MPU must perform idle cycles or other operations. Next instruction must be written after ensuring that BF is "0".

Busy Flag is read when RS=0 and RW=1 at DB7 pin (see Table 1). Reading BF procedure is used only to check the controller state and it's not an instruction, i.e. it doesn't lock input registers.

4- and 8-bit interface bus

The An6870 can operate with 4- or 8-bit interface bus. Bus width is selected by DL bit of Function Set instruction (see part 2.10).

- In 8-bit mode (DL=1) all 8 bits are used. Data is strobed by E signal. Instructions start executing at the E fall, and BF sets to "1" (see Fig.2).
- In 4-bit mode (DL=0) only 4 bits (DB4-DB7) are used for exchanging data with MPU. DB0-DB3 bits are not used (pull up to VDD). In 4-bit interface bus mode, instructions and data are transmitted in two passes, corresponding to two E pulses (see figure 3). The four high order bits (DB4 to DB7 for 8-bit operation) are transferred before the four low order bits (DB0 to DB3). Internal data selector multiplexes high and low 4-bit data groups of register, switching at E fall. Instruction writing is complete and BF is set to "1" after the second E pulse. BF must be checked after the second E pulse of instruction.

  Thus, each instruction should be accompanied with strictly two E pulses. If this condition is violated, then the sequence of data following may be broken. In this case the even and the odd 4-bit data groups of the register exchange their places. Single E pulse, owing to MPU synchronization loss or a noise influence, may break all further functioning of the controller.

  To prevent this situation, the controller has the interface synchronization function, which provides the correct order of data following through 4-bit bus: any change of both RS or RW signals resets the selector of the data to the initial status (see figure 3). Also, it is forbidden to change RS and RW status during submission of the instruction between E pulses.

2.2. Standard and Extended modes

The An6870 has XMODE pad that allows to control access to some extended functions (see Table 2). The XMODE pad has internal pull up to VDD, therefore, if the XMODE pad is not connected, it has "1" state. The customer may select additional function set for both XMODE states (see part 3.5 "Controller mask option" and Order Form in Appendix 1).

Table 2. Standard and Extended modes

XMODE	Mode	Characteristics
1 or NC*	Standard (compatible)	Mode with standard functions available. Some of Extended functions may be enabled in Standard mode specified by Order Form.
0	Extended	Mode with Extended functions, specified by Order Form : • using of second CGROM page for 5x8 dot characters or 2 pages with software switching, • underline cursor blinking, • display inversion controlling.

*NC-not connected

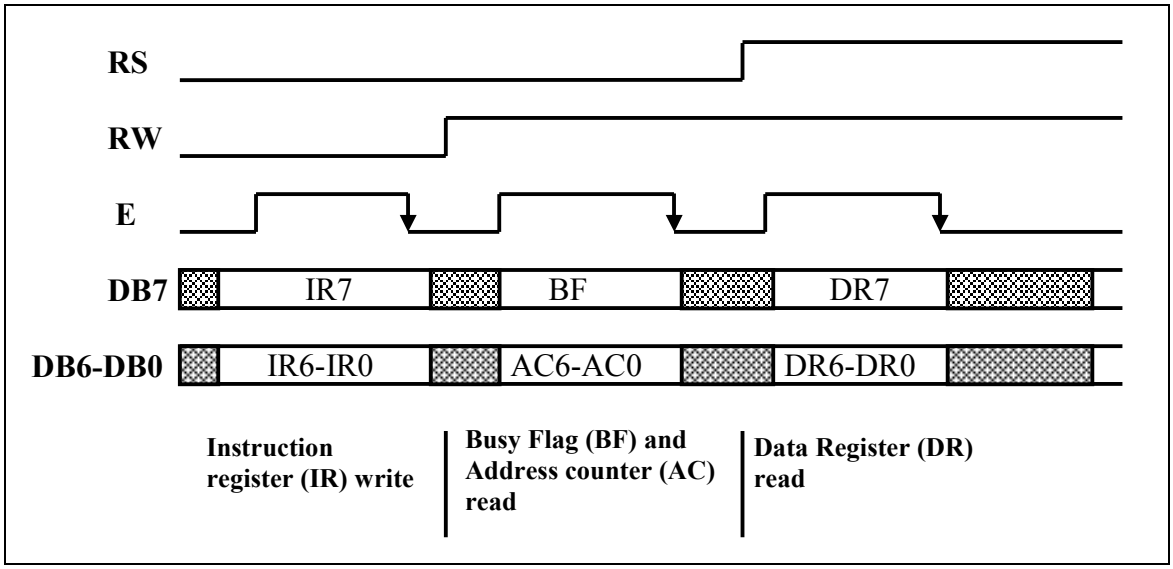


Figure 2. Example of 8-bit interface operation.

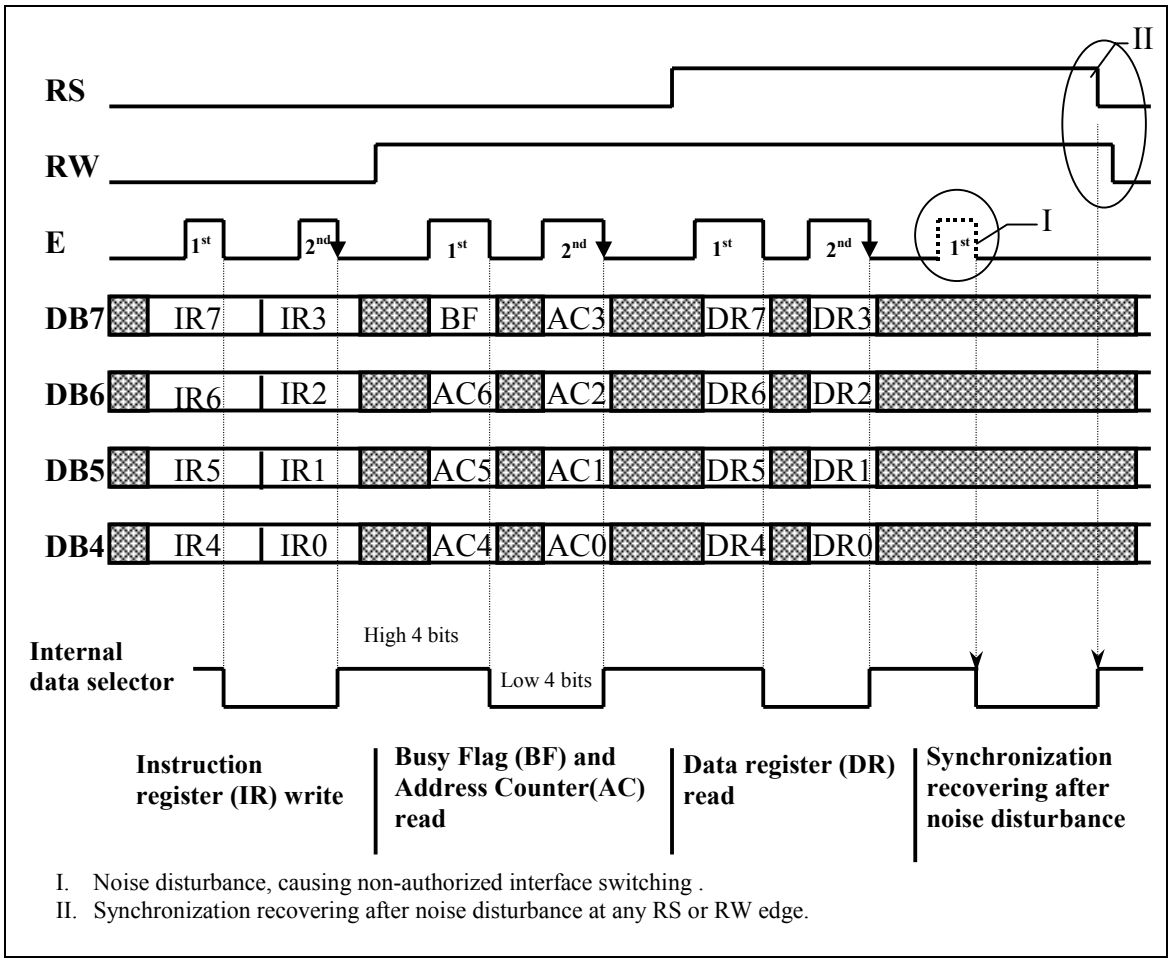


Figure 3. Example of 4-bit interface operation.

2.3. One- and two-line display

The controller can display characters in one or two lines. The number of lines is selected by Function Set instruction.

In one-line mode the controller displays characters from single DDRAM address range from 0 to 79 (4Fh). COM[1..8] lines are used for 5x8 dot characters, COM[1..11] lines are used for 5x11 dot characters.

In two-line mode the controller displays characters in two lines accordingly:

- DDRAM address range from 0 to 39 (27h) for the first line (COM[1..8]),
- DDRAM address range from 64 (40h) to 103 (67h) for the second line (COM[9..16]).

Correspondence between DRAM addresses and character positions in one-line mode and example of cursor displaying in current display position, are shown in Fig. 4, 5.

Correspondence between DRAM address and character positions in two-line mode and example of cursor displaying in current display position, are shown in Fig. 6, 7.

2.4. Address Counter (AC)

The current memory address (DDRAM and CGRAM), and cursor position are determined by Address Counter (AC). AC has reset to 0, setting a given state, increment and decrement functions.

AC resets to 0 when Display Clear and Return Home instructions are executed.

Desired AC value is set by Set DDRAM Address and Set CGRAM Address instructions. In this case the new address value is written into AC from Instruction Register (IR). Selection of memory type (DDRAM or CGRAM) is also made by these instructions.

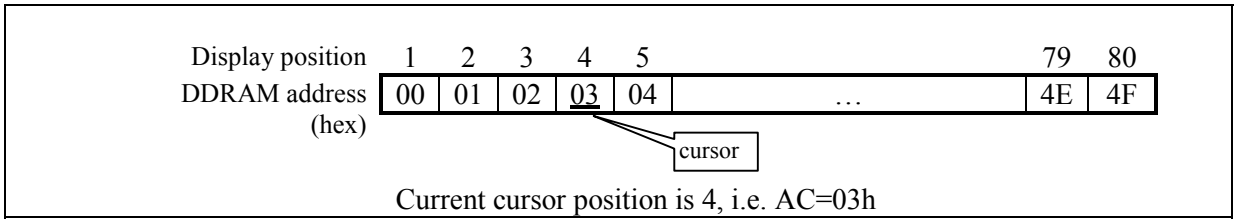


Figure 4. One-line display without shifting.

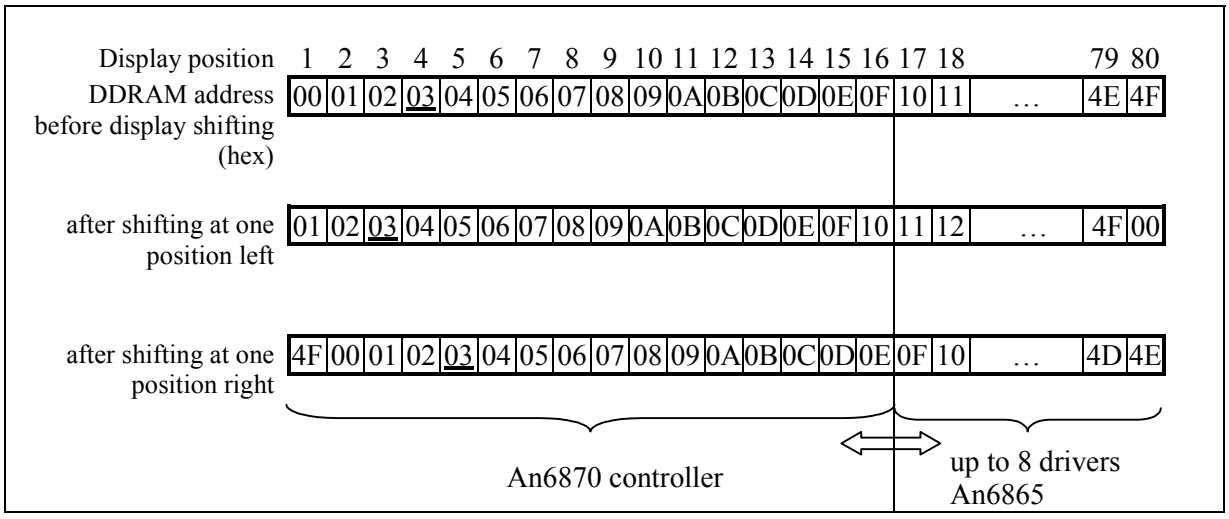


Figure 5. Display shifting in one-line mode.

Incrementing or decrementing of AC address value is made by following instructions:

- Memory read/write operations. Incrementing or decrementing is determined by ID bit of "Set Entry Mode" instruction (see part 2.10 "Instructions description").
- Cursor shift. This instruction also defines shift direction.

Count order of AC is defined by number of display lines (N bit of Function Set instruction) and accessed memory type (DDRAM or CGRAM).

While accessing to CGRAM, AC operates as complete 7-bit reversible counter without limitations (0 to 127). Only 6 bits are used for CGRAM addressing.

While accessing to DDRAM, the count order is following:

- for one-line mode:
  - incrementing: 0, 1, 2, … 78, 79, 0, 1, 2…
  - decrementing: 0, 79, 78, 77, … 2, 1, 0, 79…
  - when AC value more than 79, the counter is incremented to 127 and then sets to 0.
- for two-line mode:
  - incrementing: 0, 1, 2, … 38, 39, 64, 65, … 102, 103, 0, 1, …
  - decrementing: 0, 103, 102, … 65, 64, 39, 38, … 2, 1, 0, 103, …
  - when AC value more than 103, the counter is incremented to 127 and then sets to 0.

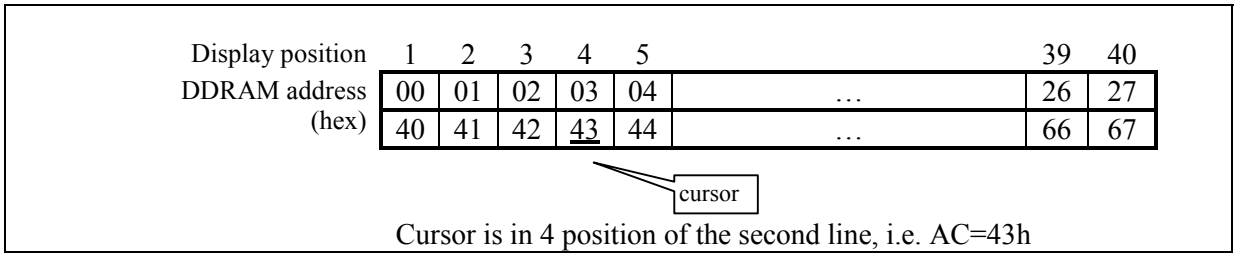


Figure 6. 2-line display without shifting.

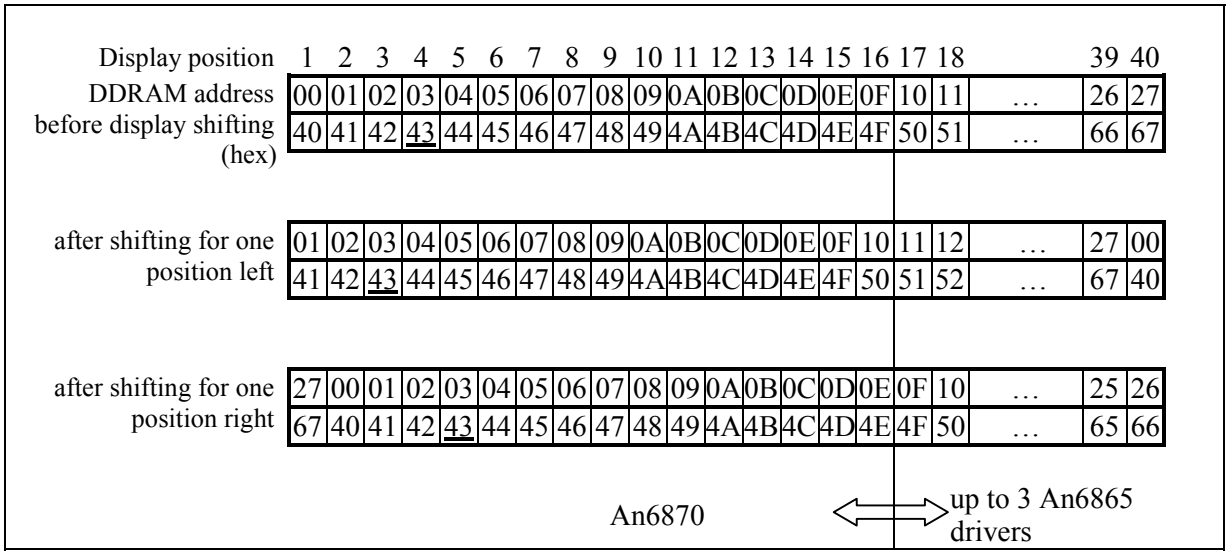


Figure 7. Display shift in 2-line mode.

2.5. Start Address Counter and display shifting

The Start Address Counter is used for display shifting. This counter contains DDRAM address, which is used in the beginning of each COM-line scanning cycle to define the initial value of Refresh Counter. The Start Address Counter has a reset function and incrementing/decrementing functions.

The counter resets to the initial state when instructions Display Clear and Return Home are executed. After resetting the character line is displayed from 0 address of DDRAM.

The counter is incremented or decremented by Display Shift instruction according to the shift direction. Count order is the same as for the AC counter (see part 2.4).

The counter has no address set function, and its state is not readable through MPU interface.

Correspondence between DDRAM address and displayed characters positions after left/right display shift in 1-line mode, is shown in Figure 5.

Correspondence between DDRAM address and displayed characters positions after left/right display shift in 2-line mode, is shown in Figure 7.

2.6. Timing Diagram

The internal controller timing diagram consists of periods, each one 5 clocks long. This is the time for transferring one character data (5-bit width) to output SEG register.

Each period contains three sequential phases of timing diagram:

1) phase of writing data to DDRAM/CGRAM and instruction execution,
2) phase of reading data from DDRAM/CGRAM to output data register of MPU interface,
3) phase of reading data from DDRAM/CGRAM/CGROM, and character displaying on LCD (i.e. display refresh).

This solution provides complete time division between memory access processes, instructions execution, and display refresh. MPU interface operates only with IR and DR registers with its own frequency independently from the slow controller timing diagram.

Phase 1 (2 clocks) provides MPU instructions execution, including instructions with memory accessing, using the address value stored in the AC. After completing data writing operation, the AC value is incremented or decremented if needed.

Phase 2 (1.5 clocks) serves for data reading from DDRAM/CGRAM to output data register DRout. Since the reading phase follows writing and instruction execution phase, data reading always occurs after address changing, if it took place during instruction execution. The following data reading instruction will allow to receive data from MPU interface, and data register will be filled with new data from the next memory address.

Phase 3 (1.5 clocks) provides display refresh and used for transferring data from CGRAM/CGROM to the data shift register. DDRAM character code, CGROM page number, and active COM number are used as CGRAM/CGROM address.

For execution of any instruction (except Display Clear) a complete pass of the 1st and 2nd phases is required. These two phases constitute Instruction Execution time, that is in a range from 3.5 to 8.5 clocks (see part 8.2). Display Clear instruction writes sequence of space characters (20h) into all 80 DDRAM addresses, which takes not more than 403.5 clocks.

There is possibility of express instructions execution under some additional conditions (see part 8.2).

Timing diagram of LCD depends on displaying mode.

In 1-line mode 80 characters of 5 bit wide can be displayed, so, the period of active COM state is 80x5=400 clocks (1.48 ms at Fosc=270 kHz). Display refresh period is:

- for font 5x8 (i.e. 8 active COM lines): 8x1.48=11.84 ms, i.e. frame frequency is ≈84.3 Hz;
- for font 5x11 (i.e. 11 active COM lines): 11x1.48=16.28 ms, i.e. frame frequency is ≈61.4 Hz.

In 2-line mode 40 characters per each line can be displayed, therefore, the time of active COM state is 40x5=200 cycles (0.74 ms at Fosc=270 kHz). Display refresh period is 16x0.74=11.84 ms, i.e. frame frequency is ≈84.3 Hz.

Note that the controller always outputs data for a full character line, but the real number of displayed characters depends on the LCD size and number of connected extension drivers.

Controller timing diagram (except MPU interface) is closured to CLK2 clock grid, that is equal to oscillator frequency F_{OSC}, therefore, the controller timing diagram changes proportionally to F_{OSC} changing.

2.7. Cursor/Character Blink control

The timer-divider with ≈0.76 sec cycle at Fosc=270 kHz is used for cursor/character blinking. Cursor or character blinking position is defined by the AC.

2.8. Power On Reset Function

The internal reset circuit automatically initializes the An6870 when the power is on. BF is kept in the busy state until the initialization is finished. Time needed for reset procedure is up to 12 ms at Fosc=270kHz.

Reset procedure performs the following functions:

- Clear Display;
- Function Set:
  DL=1, 8-bit interface*),
  N=0, 1-line display*),
  F=0, 5x8 dot character format*);
  P=0, Select of the first CGROM page, if software page control is enabled;
  I=0, Inversion is off, if inversion control is enabled;
- Display on/off:
  D=0, Display is off,
  C=0, Cursor is off,
  B=0, Blinking is off;
- Entry Mode Set:
  I/D=1, address increment mode,
  S=0, display shift disable.

*) Note: Initial state of DL, N, F bits of Function Set instruction can be defined by the Customer at the mask option order (see part 3.5. "Controller mask option").

The timer used for the initial reset procedure allows to obtain a stable result at VDD rising time up to 20 ms. However, if electrical characteristics of the device don't satisfy the conditions in part 6.3 "Power on conditions when using internal reset circuit", or if VDD voltage influence occurs, then the reset procedure may fail and cause an initialization error. In this case, it's possible to perform the initialization by instruction (see part 5.1 "Initialization by Instruction").

2.9. Instruction execution

An6870 has only two program accessible registers –instruction register (IR) and data register (DR). The number of register states and two control signals (RW – Read/Write and RS – Register Select) is determined by instruction set (Table 3). The instruction set may be divided into 4 categories:

- determination of the controller operation mode (display format, interface bus width etc.);
- setting the internal memory address and cursor position;
- transferring data between internal memory and MPU;
- service functions executing (Display Clear, Cursor Move etc.).

Usually most of executing instructions are data transferring instructions. To speed-up memory loading, the controller has an autoincrement memory address function. At that, the controller can also shift display automatically, which minimizes the number of instructions, for example, in case the cursor

reaches the end of display.

For correct controller functioning, before each instruction writing MPU must ensure that the previous instruction is completed and that interface registers are free. This can be made in two ways:

- By checking Busy Flag until its sets to 0. It's the most efficient way (see Figure 8 and 9).
- By time delay between instruction write, exceeding the maximum previous instruction execution time (see Table 3). It's a simple and slow method, but it is usable when data reading from the controller is never used (RW is fixed to 0). 4-bit interface synchronization function ensures maximum reliability of the controller operation with using only 6 interface lines (DB[7:4], E, RS).

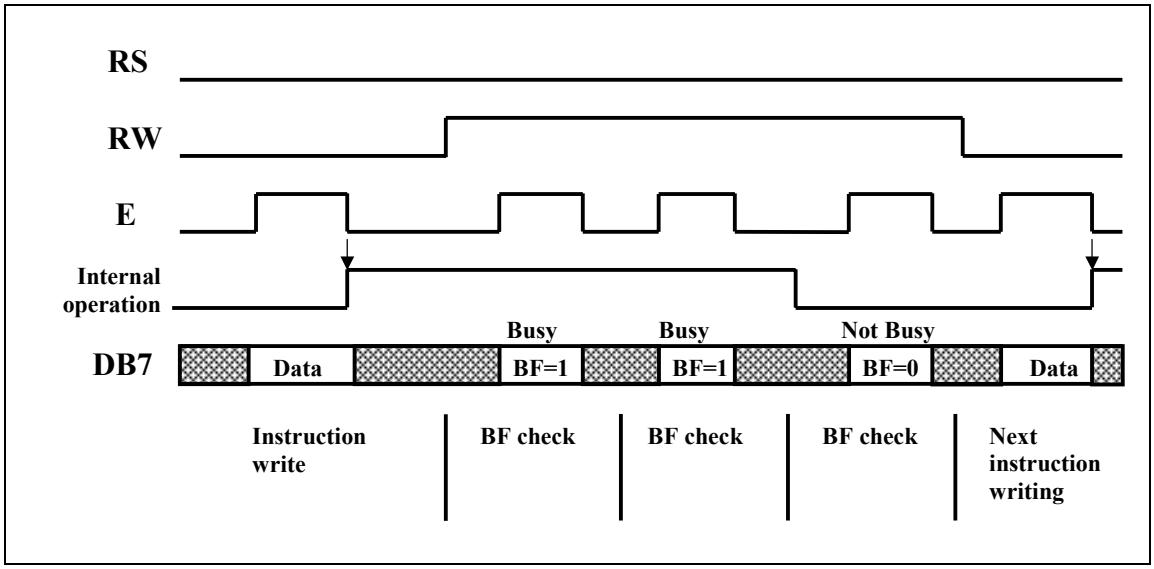


Figure 8. Example of instruction writing with Busy Flag check in 8-bit interface mode.

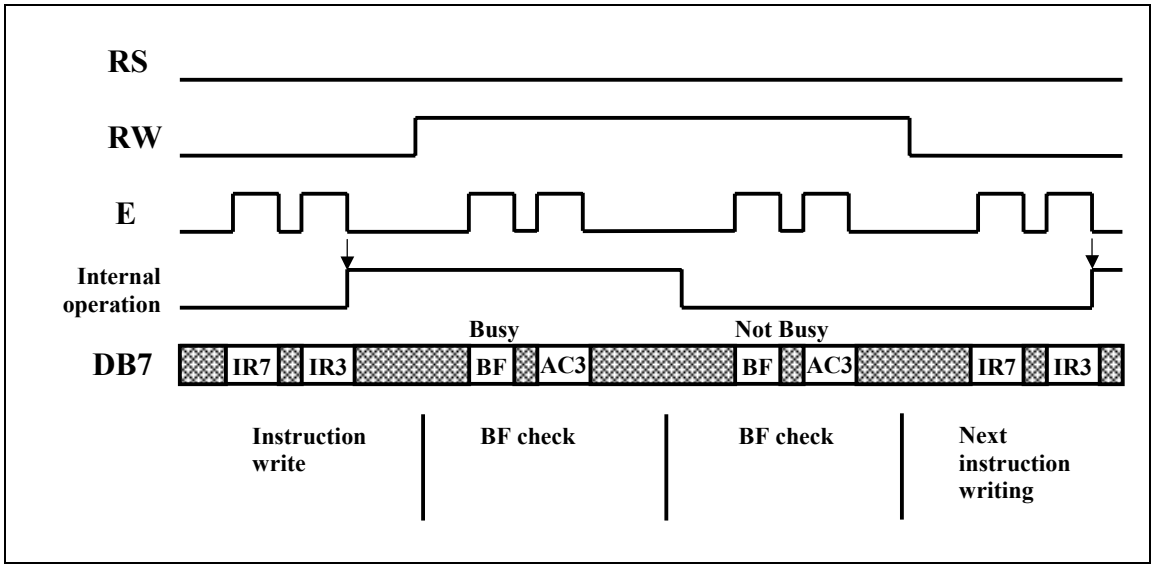


Figure 9. Example of instruction writing with Busy Flag check in 4-bit interface mode.

Table 3. Instructions

Instruction	Code										Description	Max exec. time (Fosc=270 kHz)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display Clear	0	0	0	0	0	0	0	0	0	**1**	Clear entire display and sets DDRAM address 0 in AC.	1,5 ms
Return Home	0	0	0	0	0	0	0	0	**1**	–	Sets AC and Display shift counter to 0. DDRAM contents remain unchanged.	31.45 µs
Entry Mode Set	0	0	0	0	0	0	0	**1**	**I/D**	**S**	Sets cursor move direction and specifies display shift (enables only for writing).	31.45 µs
Display on/off Control	0	0	0	0	0	0	**1**	**D**	**C**	**B**	Sets entire display (D), cursor (C) and blinking of cursor position character (B) on/off.	31.45 µs
Cursor or Display Shift	0	0	0	0	0	**1**	**S/C**	**R/L**	–	–	Moves cursor (C) and shift display (S) without changing DDRAM contents left or right (R/L).	31.45 µs
Function Set	0	0	0	0	**1**	**DL**	**N**	**F**	**P*)**	**I*)**	Set Interface data length (DL), number of display lines (N), character font (F), current page number (P), and inversion mode (I).	31.45 µs
Set CGRAM Address	0	0	0	**1**	**A_{CG}**	**A_{CG}**	**A_{CG}**	**A_{CG}**	**A_{CG}**	**A_{CG}**	Sets CGRAM address. CGRAM data is send and received after this setting.	31.45 µs
Set DDRAM Address	0	0	**1**	**A_{DD}**	**A_{DD}**	**A_{DD}**	**A_{DD}**	**A_{DD}**	**A_{DD}**	**A_{DD}**	Sets DDRAM address. DDRAM data is send and received after this setting.	31.45 µs
Read Busy Flag and Address	0	**1**	**BF**	**AC**	**AC**	**AC**	**AC**	**AC**	**AC**	**AC**	Reads BF and AC. This procedure do not blocking controller interface.	0 µs
Write data to CGRAM or DDRAM	**1**	**0**	**Write data**								Writes data to CGRAM or DDRAM.	31.45 µs
Read data from CGRAM or DDRAM.	**1**	**1**	**Read data**								Reads data from CGRAM or DDRAM.	31.45 µs

I/D: 1- Increment, 0- decrement;
S: 1- display shift enable when write to DDRAM;
D: 1- display is on, 0- display is off;
C: 1- cursor is on, 0- cursor is off;
B: 1- blinking is on, 0- blinking is off;
S/C: 1- Display shift, 0- cursor shift;
R/L: 1- Shift to the right, 0- Shift to the left;
DL: 1- 8-bit interface, 0- 4-bit interface;
N: 1- two-line display, 0- one-line display;
F: 1- font 5x11, 0- font 5x8;
P: 1- Second CGROM page, 0- First CGROM page;
I: 1- Display inversion is on, 0- Display inversion is off;

DDRAM – Display Data RAM.

CGRAM – Character Generator RAM.

A_{CG} – 6-bit CGRAM address.
A_{DD} – 7-bit DDRAM address.
AC – Address Counter for CGRAM and DDRAM addressing.
BF: 1 - Internally operating, 0 - Instructions acceptable.

– indicates no effect.
*) Extended function. Defined by Mask option (version) of controller and XMODE state

2.10. Instructions

Display Clear

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Display Clear writes space code 20h (character pattern for character code 20h must be a blank pattern) into all DDRAM addresses. Then it sets DDRAM address 0 into the address counter, and returns the display to its initial status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D bit to 1 (increment mode) in entry mode. S bit of entry mode does not change.

Return Home

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	0

Return Home sets DDRAM address 0 into the Address Counter, and returns the display to its initial status if it was shifted. The DDRAM contents do not change. According to this settings the cursor returns to the initial position, i.e. to the left edge of the display (in the first line if display in the 2-line mode).

Entry Mode Set

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	ID	S

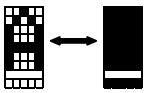
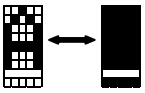
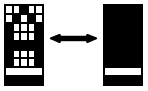
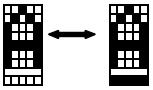
I/D: Incrementing (I/D=1) or decrementing (I/D=0) the DDRAM address by 1 when a character code is written into or read from DDRAM.
The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CGRAM.
S: When the character code is being written to DDRAM, the entire display is shifted either to the right (I/D=0) or to the left (I/D=1) when S is 1. The display does not shift if S is 0.
If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DDRAM. Also, writing into or reading out from CGRAM does not shift the display.

Display on/off

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DDRAM, but can be displayed instantly by setting D to 1.
When the display off, the repeating memory access for display refresh is absent and consumption current is decreased.
C: The cursor is displayed when C is 1 and not displayed when C is 0 in position corresponding to the AC. The cursor is displayed using 5 dots in the 8th line for 5x8 dot character font selection and in the 11th line for the 5x11 dot character font selection.
B: The character indicated by the cursor blinks when B is 1.
The cursor blinking mode is an extended function, and its use depends on chip version and XMODE state. For C=1 and B=1 case cursor blinking enable allows to obtain more effective view, than character blinking when the cursor is permanent on (see Table 4).

Table 4. Cursor displaying and character blinking modes

C	B	Cursor blink disable	Cursor blink enable
0	0	 Cursor is off, blink is off	 Cursor is off, blink is off
0	1	 Cursor is off, character blink	 Cursor is off, character blink
1	0	 Cursor is on, blink is off	 Cursor always on, blink is off
1	1	 Cursor always on, character blink	 Cursor blink

Cursor and Display Shift

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Cursor and Display Shift instruction shifts the cursor position or entire display to the right or left without changing DDRAM data (table 5). This function is used to correct or search the display. When display is shifting, cursor position follows to the display move.

In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line and vice versa. Note that the first and second display lines shift at the same time. When the display is shifted repeatedly, each line moves only horizontally. The characters in the second display line do not shift into the first line (see Figure 7).

The address counter (AC) contents will not change if the display shift is performed.

Table 5. Cursor and Display Shift modes

S/C	R/L	Description
0	0	Cursor moves left (AC decrement by 1)
0	1	Cursor moves right (AC increment by 1)
1	0	Display shift to left (start address counter increment by 1)
1	1	Display shift to right (start address counter decrement by 1)

Function Set

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	P	I

DL: Sets the interface data length. Data is transferred in 8-bit lengths (DB7-DB0) when DL=1, and in 4-bit lengths (DB7-DB4) when DL=0. When 4-bit length is selected, data must be transferred in two passes.

N: Sets the number of display lines.

F: Sets the character font.

Table 6. Function set modes

N	F	Display lines	Font size	Duty cycle	Notes
0	0	1	5x8	1/8	
0	1	1	5x11	1/11	
1	*	2	5x8	1/16	displaying 2 lines of 5x11 characters is impossible.

* -no effect.

P: Select of CGROM page: P=0 – the first page, P=1 – the second page. P bit allows to select CGROM page in the An6870 with the software support.

Two CGROM pages is an extended function in the An6870 controller. Possibility of the second page selection depends on chip version and XMODE state.

The following second CGROM page selections are possible:

- the second page is disabled, access to the first page at any case;
- page selection only by XMODE signal ("fixed" hardware selectable pages). In the standard mode the first page is selected by default (XMODE=1), in the extended mode (XMODE=0) the second page is selected. Software page selection is disabled, P bit has no effect;
- In the standard and/or extended mode software page selection is enabled, which allows to extend system functionality with the MPU software support.

I: Display inversion on/off. At I=1 black pixels become white (transparent). Inversion mode with back lighting allows to obtain "Information Board" view with bright characters on the black (dark) background.

Display inversion is an extended function, and its use depends on chip version and XMODE state.

Main features of Display Inversion function are the same as for Page Selection function (see above): disable, switching on/off by XMODE signal or software control.

Set CGRAM address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC[5]	AC[4]	AC[3]	AC[2]	AC[1]	AC[0]
				MSB					**LSB**

Set CGRAM address instruction writes 6-bit CGRAM address into the AC. After this instruction execution CGRAM is set as memory for reading/writing data.

Set DDRAM address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC[6]	AC[5]	AC[4]	AC[3]	AC[2]	AC[1]	AC[0]
			HSB						**LSB**

The instruction sets 7-bits DDRAM address into the AC. After this instruction execution DDRAM is set as memory for reading/writing data.

In 1-line mode (N=0) DDRAM address AC[6..0] must be in 00h-4Fh (0-79) range. In 2-line mode (N=1) DDRAM address AC[6..0] must be in 00h-27h (0-39) range for the first line and in 40h-67h (64-103) range for the second line.

CMID can be found in DDRAM address range 78h-7Fh (120-127, see part 3.4).

Read Busy Flag and Address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC[6]	AC[5]	AC[4]	AC[3]	AC[2]	AC[1]	AC[0]
			MSB						**LSB**

Read Busy Flag and Address instruction reads the BF indicating that the system is now internally executing the previous instruction. If BF=1, the internal operation is in process. The next instruction will not be accepted until BF is reset to 0. MPU must check the BF status before writing the next instruction. Simultaneously AC value at DB6-DB0 can be read by MPU. The address format is the same as for Set CGRAM/DDRAM Address instructions.

Note, that AC can change during execution (i.e. BF=1) of some instructions, such as data read/write, cursor move etc. It is impossible to fix the moment of AC change relatively to E fall, but it has a fixed time interval till changing BF state to 0. This interval can be used for accurate estimation of oscillator frequency (see part 8.4). Read BF procedure is used only to determine the controller status and it is not an instruction, because it doesn't change the controller state (executing time is 0).

Write Data to CGRAM or DDRAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
		MSB							**LSB**

Write Data to CGRAM or DDRAM instruction writes 8-bit binary data to CGRAM or DDRAM.

The address is determined by the previous specification of the CGRAM or DDRAM address setting. After a write the address is automatically incremented or decremented by 1 according to the I/D bit of entry mode. Also it is possible to shift entire display backward when data writing to DDRAM (not CGRAM!), if this operation enabled by S bit of entry mode.

Read Data from CGRAM or DDRAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
		MSB							**LSB**

The Read Data from CGRAM or DDRAM instruction reads 8-bit binary data D[7..0] from CGRAM or DDRAM at AC address into data bus interface.

Reading data from DDRAM/CGRAM is realized in two stages. First, after any instruction execution CGRAM/DDRAM data is put into output data register (DRout). This is guaranteed that data in the DRout is always from the last address, even it has been changed during the last instruction execution. At high E level data from DRout is transferred to data bus interface. Then at E fall the controller performs AC incrementing or decrementing during instruction execution according to I/D bit of entry mode. At that, reading data from next memory address into DRout is performed.

Automatical AC incrementing or decrementing imply that the last written data cannot be verified immediately by the Read instruction. If the verification is needed, executing the address set or cursor move instructions must be performed before reading data.

When data reading, the display is not shifting.

3. INTERNAL CONTROLLER MEMORY

3.1. Display Data RAM (DDRAM)

DDRAM stores display data represented in 8-bit character codes.

In read/write mode, access to DDRAM is made at the current AC address. DDRAM addressing depends on the number of display lines:

- in 1-line mode address, range from 0 to 79 is used,
- in 2-line mode, the following address ranges are used (see part 2.4):
  - 0-39 for the first line,
  - 64-103 for the second line.

At display refresh, the code read from the DDRAM combined with the current COM number and page number is used to generate CGROM/CGRAM address. Character pattern information from CGROM/CGRAM is used for displaying characters on LCD.

3.2. Character Generator ROM (CGROM)

CGROM pattern is programmed by mask option during manufacture. There are 2 available font sizes: 5x8 and 5x11 dots.

8-bit character code allows to display simultaneously up to 256 characters from character pattern table (see Appendix 5). Each character code is composed from 4-bit column address and 4-bit row address. 240 or 248 codes may be assigned to the CGROM, correspondingly 16 or 8 codes remain for the CGRAM.

The CGROM consists of 248 character cells of 5x16 size. In each cell it's possible to place two 5x8 dot characters or one 5x11 dot character. The 5x8 dot character set forms two CGROM pages accessible by P bit of Function Set instruction and XMODE signal (depends on the controller mask option). 5x11 dot characters can not be coded in two pages, therefore, they have only one set and they are displayed equally for both pages.

There are some differences in address generating for 5x8 dot and 5x11 dot characters (see tables 7 and 8). Therefore, the controller contains special circuits - comparators of 4 high order bits of the address that defines code range for two-page table region with 5x8 characters: Amin ÷ Amax.

Inside the Amin÷Amax range it's possible to select 5x8 character with P bit (page number) and XMODE state. Outside the Amin÷Amax range it's possible to select characters only from one page, which allows to code one set of 5x8 or 5x11 characters.

Since only 4 high order bits of the address (or character code) are compared, the table may be divided into one-page and two-page parts, multiplicity equals strictly 16 (entire column). For example, for S00 coding Amin=1h and Amax=Dh, which allows to code 208 5x8 characters per each of two pages (10h-DFh), and 32 5x11 characters (E0h-FFh).

For the Customer's new mask option and page control possibilities see part 3.5 "Controller mask option", for released options see Appendix 5.

Note that in 1-line mode with 1/8 duty (N=0 и F=0), and in 2-line mode, 5x11 dot characters are displayed in a truncated form: only 8 upper COM-lines are displayed. On the other hand, in 1/11 duty mode (i.e. at 11 active COM-lines) 5x8 characters at two-page coding are supplemented with spaces in 9, 10 and 11 COM-lines, thus, providing correct displaying though character presence on the next page (see Table 8).

The An6870 also has a capability to readdress 08h-0Fh codes to CGROM, which is assigned for replication of 00h-07h CGRAM codes. The corresponding function is enabled by the controller mask option according to the Customer's request (see part 3.5). In this case, maximum CGROM capacity is up to 248 characters at each of two pages, 496 characters in two pages in 08h-FFh code range.

3.3. Character Generator RAM (CGRAM)

The user can write into CGRAM his own character patterns: 8 characters 5x8 dots or 4 characters 5x11 dots. Correspondence of CGRAM addresses and character codes is shown in Table 9 for 5x8 dots characters and in Table 10 for 5x11 dot characters.

CGRAM cell, which contains information about one 5x8 character occupies 8 bytes. Each byte contains information about one character line; only 5 low order bits (D4-D0) are used for displaying, 3 high order bits (D7-D5) are not used. The CGRAM size is 64 bytes; it is possible to write 8 characters 5x8 dots.

When writing 5x11 characters, each character occupies two 8-byte CGRAM cells. In the second cell 9, 10, 11 character lines are coded. Information in the next 5 bytes is not displayed and may contain general purpose data. CGRAM 5x11 dot character codes will be numbered every other one in 00h-07h code range. For example, if the first character is written in CGRAM from cell 0 occupying cells 0 and 1, it is possible to use codes 00h, 02h, 04h and 06h to display such 4 characters.

Note: When using 5x11 font mode, 5x8 characters must also be coded in 11 lines with spaces in 9, 10, and 11 character lines, because function of automatical space filling, used in 2-page CGROM code table, does not work with CGRAM.

In the standard chip version 16 codes are used for CGRAM. CGRAM characters repeat twice – for codes 00h-07h and 08h-0Ah. At that, the D3 bit of character code is not used for CGRAM addressing.

For advanced possibilities, the D3 bit (address A7, see Table 9) may be used for CGROM/CGRAM address sharing. Codes 00h-07h remain for CGRAM. 8 additional codes (08h-0Fh) pass to CGROM, thus, increasing the total character numbers up to 248.

In Tables 9 and 10 there are complete addresses used to address CGROM/CGRAM, and corresponding AC addresses used for access through the MPU interface.

Table 7. CGROM addressing and 5x8 dot character coding

CGROM Address												Data					
Character code								P	COM[1..8]								
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_4	Q_3	Q_2	Q_1	Q_0	
								0	0	0	0	**1**	0	0	0	0	
								0	0	0	1	**1**	0	0	0	0	
								0	0	1	0	**1**	0	**1**	**1**	0	
								0	0	1	1	**1**	**1**	0	0	**1**	**First page**
								0	1	0	0	**1**	0	0	0	**1**	
								0	1	0	1	**1**	0	0	0	**1**	
								0	1	1	0	**1**	**1**	**1**	**1**	0	
0	1	1	0	0	0	1	0	0	1	1	1	0	0	0	0	0	← cursor position
								1	0	0	0	**1**	0	0	0	0	
								1	0	0	1	**1**	0	0	0	0	
								1	0	1	0	**1**	**1**	**1**	**1**	0	
								1	0	1	1	**1**	0	0	0	**1**	**Second page**
								1	1	0	0	**1**	0	0	0	**1**	
								1	1	0	1	**1**	0	0	0	**1**	
								1	1	1	0	**1**	**1**	**1**	**1**	0	
								1	1	1	1	0	0	0	0	0	← cursor position

Notes:
1. Character code, corresponding to the addresses A_{11}-A_4, is chosen from DDRAM (D7-D0) according to the character position on the display.
2. P (address A_3) –CGROM page number.
3. Addresses A_2-A_0 –COM[1..8]-line number.
4. Pixel is "on" corresponding to "1" in CGROM.

Table 8. CGROM addressing and 5x11 dot character coding

CGROM Address												Data					
Character code								COM[1..11]									
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_4	Q_3	Q_2	Q_1	Q_0	
								0	0	0	0	**1**	0	0	0	0	
								0	0	0	1	**1**	0	0	0	0	
								0	0	1	0	**1**	0	**1**	**1**	0	
								0	0	1	1	**1**	**1**	0	0	**1**	**First page**
								0	1	0	0	**1**	0	0	0	**1**	**or**
								0	1	0	1	**1**	0	0	0	**1**	**Second page**
								0	1	1	0	**1**	**1**	**1**	**1**	0	
0	1	1	0	0	0	1	0	0	1	1	1	0	0	0	0	0	
								1	0	0	0	0	0	0	0	0	At 1/11duty 5x8 character is supplemeted with "0" in 9, 10 and 11 lines
								1	0	0	1	0	0	0	0	0	
								1	0	1	0	0	0	0	0	0	←cursor position
								1	0	1	1	*	*	*	*	*	
								1	1	0	0	*	*	*	*	*	
								1	1	0	1	*	*	*	*	*	
								1	1	1	0	*	*	*	*	*	
								1	1	1	1	*	*	*	*	*	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	
								0	0	0	0	0	0	0	0	0	
								0	0	0	1	0	0	0	0	0	
								0	0	1	0	0	**1**	**1**	0	**1**	
								0	0	1	1	**1**		0	**1**	**1**	
								0	1	0	0	**1**	0	0	0	**1**	
								0	1	0	1	**1**	0	0	0	**1**	
								0	1	1	0	0	**1**	**1**	**1**	**1**	
1	1	1	1	0	0	0	1	0	1	1	1	0	0	0	0	**1**	
								1	0	0	0	0	0	0	0	**1**	
								1	0	0	1	0	0	0	0	**1**	
								1	0	1	0	0	0	0	0	0	←Cursor position
								1	0	1	1	*	*	*	*	*	
								1	1	0	0	*	*	*	*	*	
								1	1	0	1	*	*	*	*	*	
								1	1	1	0	*	*	*	*	*	
								1	1	1	1	*	*	*	*	*	

Notes:
1. Character code, corresponding to the addresses A_{11}-A_4, is chosen from DDRAM (D7-D0) according to the character position on the display.
2. Addresses A_3-A_0 – COM[1..11]-line number.
3. 5x8 characters from two-page area (Amin÷Amax) are supplemented with "0" in COM[9..11]-lines.
4. Characters from one-page area out of the address range (Amin÷Amax) occupy all 11 lines.
5. Data in COM[12..16]-lines are not displayed (sign *).
6. Pixel is "on" corresponding to "1" in CGROM.

Table 9. CGRAM addressing for 5x8 dot characters

CGRAM selection sign					CGRAM Address								Data								
Character code								COM[1..8]													
					AC_5	AC_4	AC_3		AC_2	AC_1	AC_0		MSB							LSB	
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	
0	0	0	0	*	0	0	0	*	0	0	0		*	*	*	1	1	1	1	0	**First character**
								*	0	0	1		*	*	*	1	0	0	0	1	
								*	0	1	0		*	*	*	1	0	0	0	1	
								*	0	1	1		*	*	*	1	1	1	1	0	
								*	1	0	0		*	*	*	1	0	1	0	0	
								*	0	0	1		*	*	*	1	0	0	1	0	
								*	1	0	0		*	*	*	1	0	0	0	1	
								*	1	0	1		*	*	*	0	0	0	0	0	← cursor position
0	0	0	0	*	0	0	1	*	0	0	0		*	*	*	1	0	0	0	1	**Second character**
								*	0	0	1		*	*	*	0	1	0	1	0	
								*	1	0	0		*	*	*	1	1	1	1	1	
								*	1	0	1		*	*	*	0	0	1	0	0	
								*	0	0	0		*	*	*	1	1	1	1	1	
								*	0	0	1		*	*	*	0	0	1	0	0	
								*	0	1	0		*	*	*	0	0	1	0	0	
								*	0	1	1		*	*	*	0	0	0	0	0	← cursor position
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…

Notes:
1. Character code, corresponding to the address A_{11}-A_4, is chosen from DDRAM (D7-D0) according to the character position on the display.
2. Addresses A_{11}-A_7 indicate CGRAM selection for display refresh (A_{11}-A_7=0000*). Address A_7 is not usually used, that means, selection of CGRAM for codes 00h-0Fh. However, it may be additionally determined, at that, A_7=0 will mean selection of CGRAM (8 codes 00h-07h), A_7=1 – selection of CGROM (8 additional codes 08h-0Fh, totally 248 CGROM characters).
3. Addresses A_6-A_4 – CGRAM character code (3 addresses, 8 characters 5x8).
4. Address A_3 – not used to display 5x8 characters.
5. Addresses A_2-A_0 – COM[1..8]-line number.
6. AC_5-AC_0 – the address counter (AC) bits while read/write data operations.
7. Lighted pixel corresponding "1" in CGRAM.
8. CGRAM Q_7-Q_5 lines are not displayed and can be used as conventional memory.

Table 10. CGRAM addressing for 5x11 dot characters

CGRAM selection sign					CGRAM Address										Data								
Character code								COM[1..11]															
					AC_5	AC_4		AC_3	AC_2	AC_1	AC_0	MSB							LSB		
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0		
0	0	0	0	*	0	0	*	0	0	0	0	*	*	*	0	0	0	0	0		
								0	0	0	1	*	*	*	0	0	0	0	0		
								0	0	1	0	*	*	*	**1**	0	**1**	**1**	0		
								0	0	1	1	*	*	*	**1**	**1**	0	0	**1**	**First character**	
								0	1	0	0	*	*	*	**1**	0	0	0	**1**		
								0	0	0	1	*	*	*	**1**	0	0	0	**1**		
								0	1	0	0	*	*	*	**1**	**1**	**1**	**1**	0		
								0	1	0	1	*	*	*	**1**	0	0	0	0		
								1	0	0	0	*	*	*	**1**	0	0	0	0		
								1	0	0	1	*	*	*	**1**	0	0	0	0		
								1	1	0	0	*	*	*	0	0	0	0	0	← cursor position	
								1	1	0	1	*	*	*	*	*	*	*	*		
								1	0	0	0	*	*	*	*	*	*	*	*		
								1	0	0	1	*	*	*	*	*	*	*	*		
								1	0	1	0	*	*	*	*	*	*	*	*		
								1	0	1	1	*	*	*	*	*	*	*	*		
0	0	0	0	*	0	1	*	0	0	0	0	*	*	*	0	0	0	**1**	0		
								0	0	0	1	*	*	*	0	0	0	0	0		
								0	0	1	0	*	*	*	0	0	**1**	**1**	0		
								0	0	1	1	*	*	*	0	0	0	**1**	0	**Second character**	
								0	1	0	0	*	*	*	0	0	0	**1**	0		
								0	0	0	1	*	*	*	0	0	0	**1**	0		
								0	1	0	0	*	*	*	0	0	0	**1**	0		
								0	1	0	1	*	*	*	0	0	0	**1**	0		
								1	0	0	0	*	*	*	**1**	0	0	**1**	0		
								1	0	0	1	*	*	*	0	**1**	**1**	0	0		
								1	1	0	0	*	*	*	0	0	0	0	0	← cursor position	
								1	1	0	1	*	*	*	*	*	*	*	*		
								1	0	0	0	*	*	*	*	*	*	*	*		
								1	0	0	1	*	*	*	*	*	*	*	*		
								1	0	1	0	*	*	*	*	*	*	*	*		
								1	0	1	1	*	*	*	*	*	*	*	*		
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	

Notes:
1. Character code, corresponding with addresses A_{11}-A_4, is chosen from DDRAM (D7-D0) according to character position on display.
2. Addresses A_{11}-A_7 are indicating selection of CGRAM for display refresh (A_{11}-A_7=0000*). Address A_7 usually not used, that means selection of CGRAM for codes 00h-0Fh. However, it may be additionally determined, A_7=0 is mean selection of CGRAM (4 codes from 00h-07h range every other one), A_7=1 – selection of CGROM (additional 8 codes 08h-0Fh, 248 CGROM characters at all).
3. Addresses A_6-A_5 – CGRAM character code (2 addresses, 4 characters 5x11).
4. Address A_4 – not used for display 5x11 characters.
5. Addresses A_3-A_0 –COM[1..11]-line number.
6. AC_5-AC_0 –address counter (AC) bits while read/write data.
7. Pixel is "on" corresponding to "1" in CGROM.
8. CGRAM Q_7-Q_5 lines and bytes 12 to 16 for each character are not displayed and can be used as conventional memory.

3.4. Chip and Mode Identifier (CMID)

The chip version and the current operation mode identifier (Chip & Mode IDentifier - CMID) gives MPU the information about the controller type being used, its functionalities, CGROM mask option, the current status and operation mode. The identifier occupies a range of DDRAM addresses from 78h up to 7Fh (120-127). To read all the bits of CMID it is necessary to set DDRAM address to 78h in the increment mode or 7Fh in the decrement mode and to read sequently 8 bytes of data. The structure of the identifier is given in table 11. Coding variants of the registered controller versions see in Appendix 6.

According to type of information, the identifier may be divided into two parts: permanent and variable. For permanent part mask programming is performed at the factory. The mask contains the chip

Table 11. CMID bits description

Address		An6870 Identificator coding								Parameter
Dec.	Hex.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
120	78h	0	1	0	0	0	0	0	1	An6870 Chip Identifier
121	79h	0	1	0	0	1	1	1	0	
122	7Ah	0	1	0	0	0	1	0	0	
123	7Bh	0	1	0	0	0	1	1	0	
124	7Ch	PF	V	V	V	V	V	V	V	CGROM mask
125	7Dh	NL	NF	FS	FF	PN	PX	IN	IX	Configuration
126	7Eh	LF	SZ	CBN	CBX	WFN	WFX	P	I	Config./Current state
127	7Fh	X	N	F	D	C	B	ID	S	Current state

Permanent part

V	CGROM characters pattern version
PF	Pages Fix mode (when 1: PN/PX - page number in Standard/Extended modes, when 0: PN/PX - page control enable in Standard/Extended modes)
NL	Number of Lines
NF	Number of Lines Fix/init
FS	Font Size (5x8 or 5x11)
FF	Font size Fix/init
PN	When PF=1 – page number in Standard mode, When PF=0 – page control enable in Standard mode
PX	When PF=1 – page number in Extended mode, When PF=0 – page control enable in Extended mode
IN	Inverse enable in Standard mode
IX	Inverse enable in Extended mode
LF	Large Font mode (1 – for version An6870A)
SZ	CGROM Size: 1 for double size (for further development)
CBN	Cursor Blink in Standard mode
CBX	Cursor Blink in Extended mode
WFN	WaveForm type in Standard mode (0- A-type, 1- B-type)
WFX	WaveForm type in Extended mode (0- A-type, 1- B-type)

Variable part

P	Current page	D	Display on/off
I	Current display inversion mode	C	Cursor on/off
X	XMODE state	B	Blinking on/off
N	Number of display lines	ID	Address Inc. or Dec. when data read/write
F	Font size	S	Display shift enable when write to DDRAM

identifier, number of CGROM mask option and flags describing availability of various extended functions in standard and extended operation modes. The variable part indicates the information on the current software controlled operation modes established by MPU instructions.

Information given by the identifier may be used by MPU software to increase its flexibility and reliability. It's very crucial in mass production of devices with mask ROM MPU. Subject to the controller version, it is possible to use one program placed in MPU ROM to produce devices with different functionalities or for the different markets (countries).

There are some typical ways of the identifier application:

- use controller type data to adjust the program for specified chip features and to distinguish the controller from analogues of other manufacturers;
- use ROM mask option data to solve language problems during the device localization in different markets (countries);
- use controller functional possibilities data for its correct use, also in combination with other functional parts of the device;
- use information of the current controller operation mode to increase total reliability of the device operation, and also for its testing and self-diagnostic.

It is supposed that this access method and identifiers will remain for all chips of dot matrix character controllers family.

3.5. Controller mask option

There are two parts in controller mask option:

- Functional mask option;
- Character Generator ROM mask.

Functional mask option allows to enable or disable extended functions in standard (XMODE=1) and extended (XMODE=0) modes. Full list of extended functions and comments is given in Order Form (see Appendix 1 and 2).

CGROM mask options contains:

- coding of the first and the second CGROM pages,
- address range for the second page (Amin-Amax),
- 08h-0Fh code range CGROM selection enabling.

The Customer specifies all the desired functions in Order Form (Appendix 1 and 2), and his own character code tables (Appendix 3 and 4), if needed. All the mask options are programmed by metal layer.

Mask options have unique 4-digit number, used in complete controller marking – An6870-xxyy. The first two digits – functional mask version, the last two digits – CGROM version. Version number is designated by ANGSTREM during the customer mask generation.

3.6. Mask option order

The order of new controller mask option is made in the following sequence:

1. The CUSTOMER develops the mask option specification and CGROM character table with help of CGROM font editor program, fills in the Order Form and sends them to ANGSTREM.
2. ANGSTREM checks correctness of the received specification, designate a 4-digit number to the new mask option, develops the appropriate coding of the controller identifier (CMID) and enters the new coding in the CAD system database.
3. ANGSTREM sends to the CUSTOMER the specification of mask option and the CGROM character table, obtained by the CAD system.
4. The CUSTOMER checks conformity of mask option parameters to his requirements and confirms their correctness.
5. ANGSTREM makes an experimental lot and send it to the CUSTOMER for testing as a part of user device.
6. After reception of the positive conclusion from the CUSTOMER, ANGSTREM begins a mass production of the controller with the new mask option.

4. LCD DRIVERS CIRCUIT

4.1. LCD interface

The LCD is a matrix consisting of lines (rows) and columns on which crossings there are active elements. Matrix rows are connected to COM [1:16] outputs, and columns - to SEG outputs of controller or extension drivers.

To display information, the multiplexing method is used, i.e. dynamic sharing of the displayed information in time. In every moment of time, information established on the controller SEG outputs is highlighted only for one active COM-line. After a time period equal to the period of line frequency, the next COM becomes active, and the appropriate information is established in SEG outputs for this COM. During the full screen refresh (frame frequency period) all COM-lines are activated according duty cycle. It is supposed, that the established pixels status is kept at least for the one period of screen update.

The controller can output three types of timing diagram: 1/8, 1/11, 1/16 duty cycle depending on the display mode (see Table 12). Denominator shows the amount of active COM-lines. Other COM-lines always remain passive, and the connected pixels – not highlighted.

Activity of COM-lines is determined by the counter-decoder which sequentially touches all COM-lines up to the maximal value determined by the appropriate display mode.

Information about displaying characters is sent to the controller SEG outputs and extension drivers outputs. The An6870 has positive display logic when "1" corresponds to the highLighted pixel located on the current active COM-line.

Examples of various LCD connection variants are given in Figures 10-14.

Table 12 Display modes

Number of lines	Font size	Number of active COM-lines	Duty cycle
1	5x8	8	1/8
1	5x11	11	1/11
2	5x8	16	1/16

4.2. CGROM output data writing to SEG shift registers

CGROM output data intended for displaying, are converted from parallel to serial form and then written into the SEG shift register with CLK2 frequency equal to oscillastor frequency F_{OSC}.

The information about displayed characters is transferred into the shift register reverse order, i.e. for each COM-line first the data for last character are transferred, then the refresh address decreases and the information for the previous character is transferred etc. (for example, see Figure 3 and 4 for one-line mode and Figure 5 and 6 for two-line mode). The number of the last character of a line, which is first loaded into the shift register, is set by the start address counter (see part 2.5 "Start Address Counter and display shifting"). The first 16 characters of a line are always displayed with the own SEG drivers (totally 80 SEG outputs). Data for these characters are received at the end of a COM-line update cycle.

After filling the shift register with the data for next COM-line, data are writing in SEG latches at CLK1 fall, and displayed onto LCD simultaneously with switching to the next COM. Then the shift register fills up with data for the next COM. Thus, a CLK1 pulse is a line frequency synchronization signal.

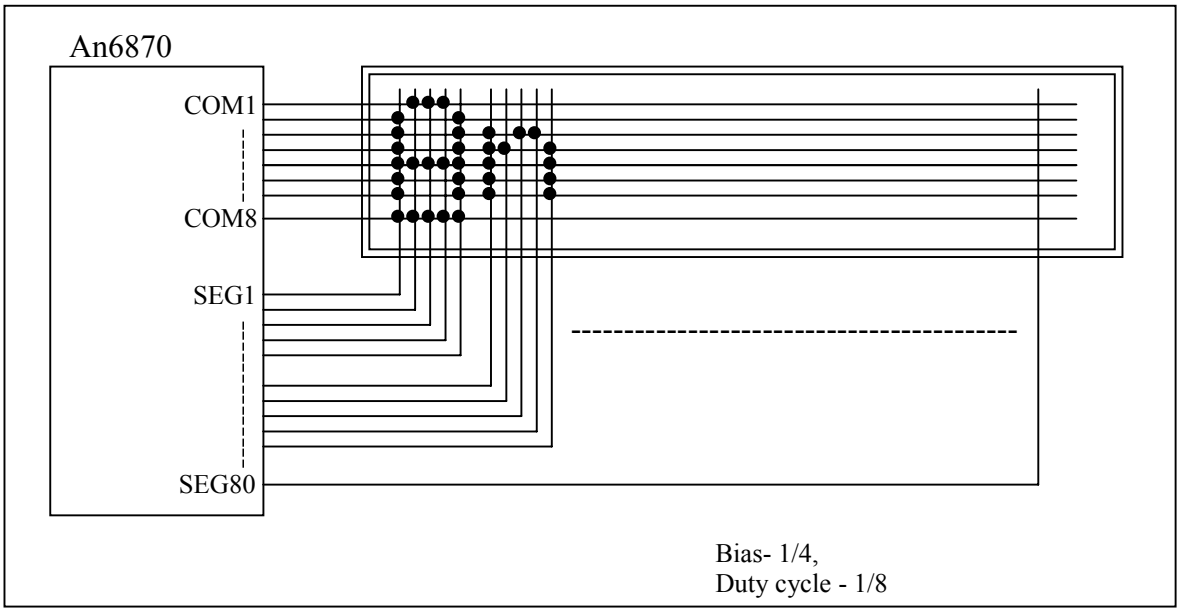


Figure 10. Example of 5x8 dots, 16 character x 1 line display.

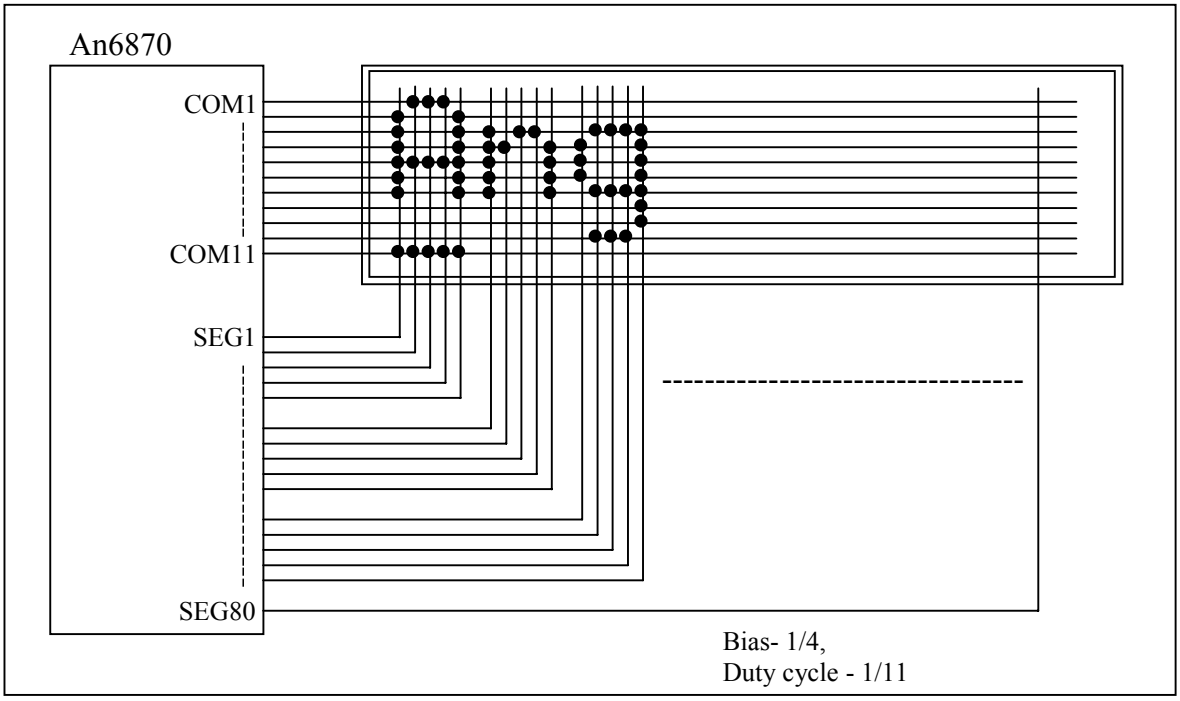


Figure 11. Example of 5x11 dots, 16 character x 1 line display.

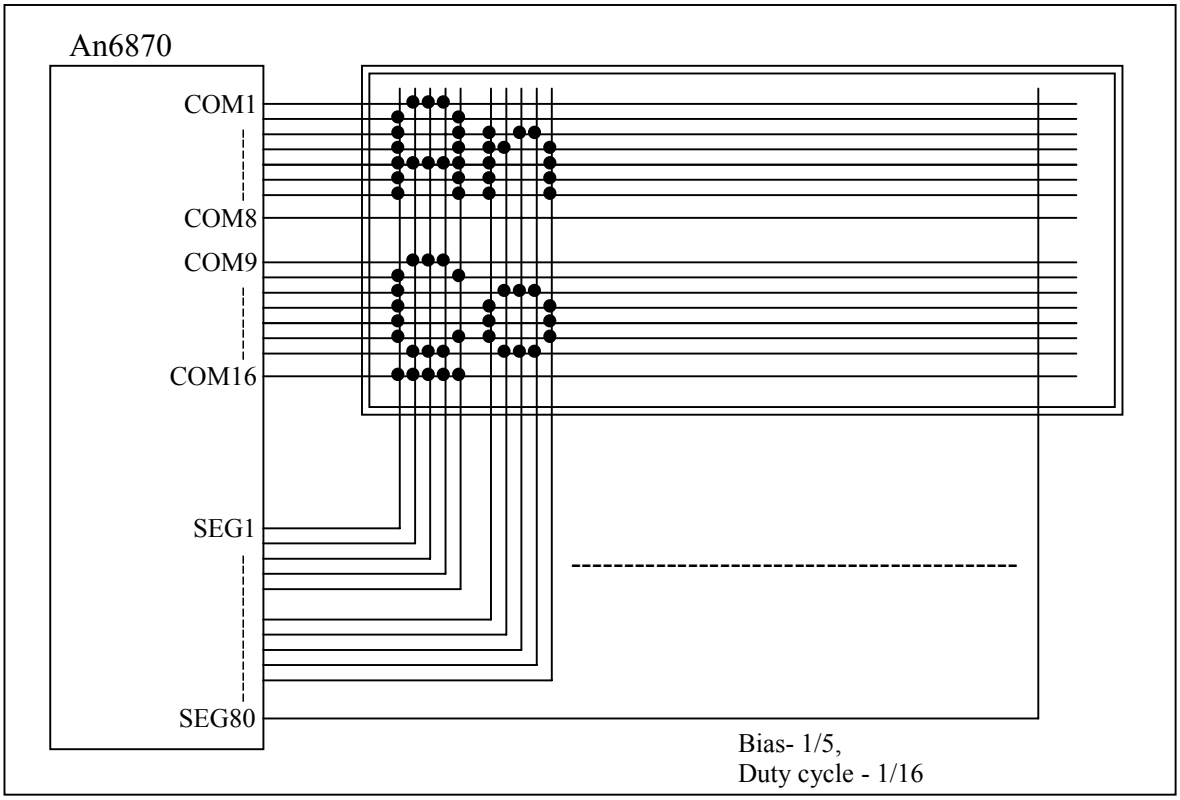


Figure 12. Example of 5x8 dots, 16 character x 2 line display (32 characters).

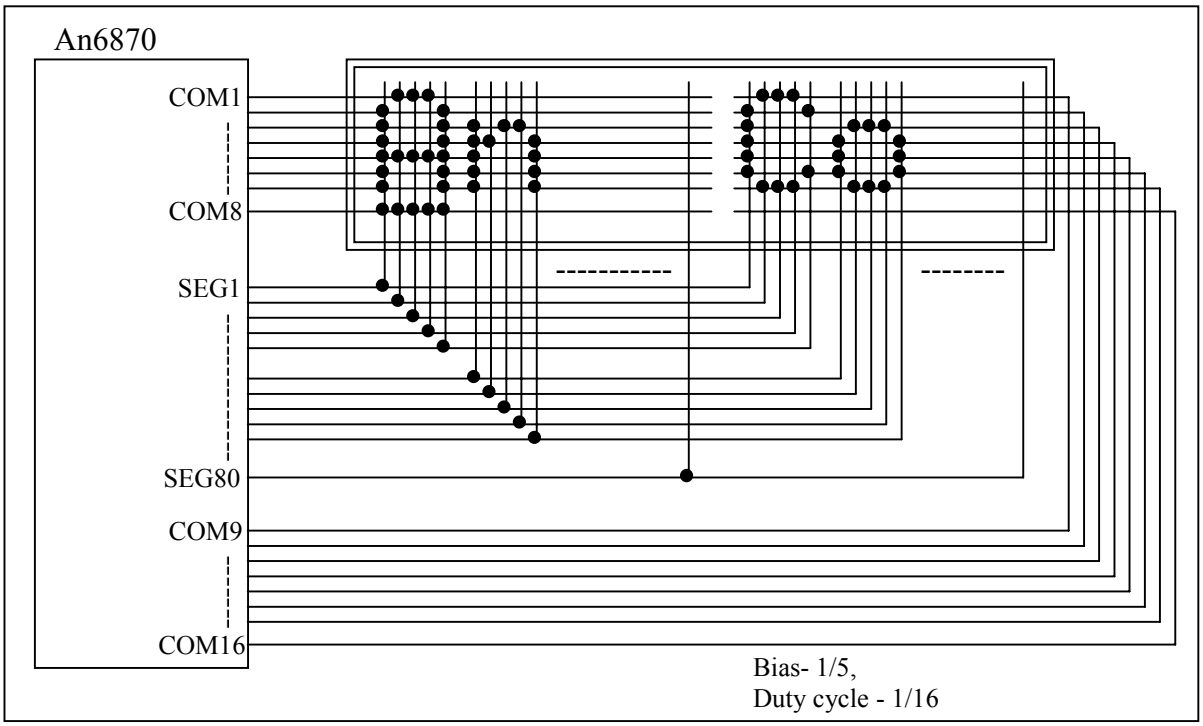


Figure 13. Example of 5x8 dots, 32 character x 1 line display (non-standard LCD layout).

4.3. Connection of the extension drivers

An6870 can display up to 16 characters in one line with internal SEG drivers. To increase number of displayed symbols, external drivers such as An6865 (40 SEG) or An6863 (80 SEG) are used. These chips contain their own SEG shift registers, which are cascade-connected to shift register output (D) increasing its length (see part 8.1).

Maximum register length and corresponding number of displayed characters are limited by COM-line refresh cycle, and they are equal to 400 for 1-line mode (80 characters per line) and 200 for 2-line mode (40 characters per line).

Extension drivers are connected through 4-bit bus interface. This interface contains D shift register output, shift data strobe CLK2, latches strobe CLK1 and alternate LCD voltage signal M.

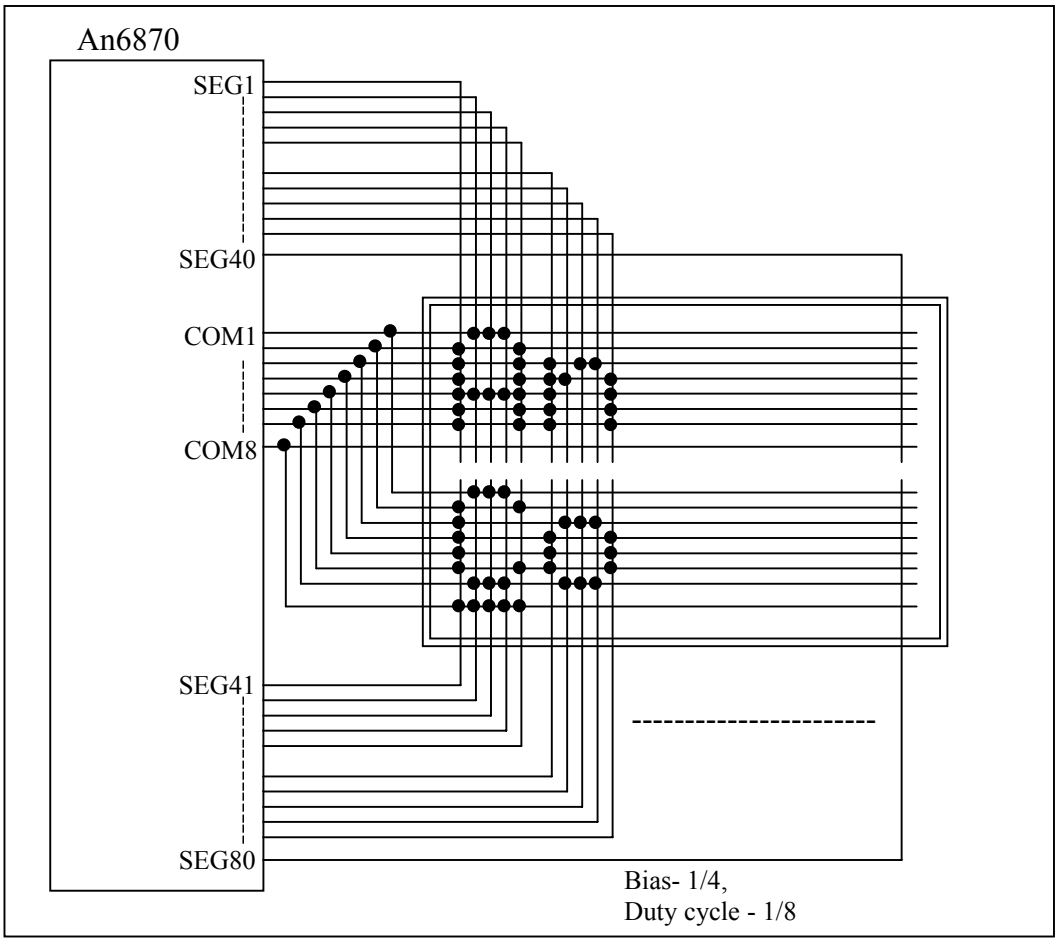


Figure 14. Example of 5x8 dots, 8 character x 2 line display (16 characters).

4.4. Power Supply for LCD Drive

COM and SEG drivers that output information directly to the LCD, form a complex multilevel timing diagram (see Figure 16-18).

Maximum voltage applied to LCD is V_{LCD}=VDD-V5. All this voltage range, with resistive divider, is split into 5 levels with 1/4 bias or into 6 levels with 1/5 bias (see Figure 12). These voltages are supplied to V1-V5 controller pins.

Each driver circuit commutates these voltages in the following way: less voltage outputs to non-lighted pixels, and entire V_{LCD} voltage outputs to lighted pixels. Because of LCD sluggishness, even a short action of high V_{LCD} voltage to activite display pixels is enough for high contrast of display image.

Table 13 Bias for LCD driving

Duty cycle	1/8, 1/11	1/16
Bias	1/4	1/5
Power supply pin	Voltage level	
V1	VDD-1/4 V_{LCD}	VDD-1/5 V_{LCD}
V2	VDD-1/2 V_{LCD}	VDD-2/5 V_{LCD}
V3	VDD-1/2 V_{LCD}	VDD-3/5 V_{LCD}
V4	VDD-3/4 V_{LCD}	VDD-4/5 V_{LCD}
V5	VDD-V_{LCD}	VDD-V_{LCD}

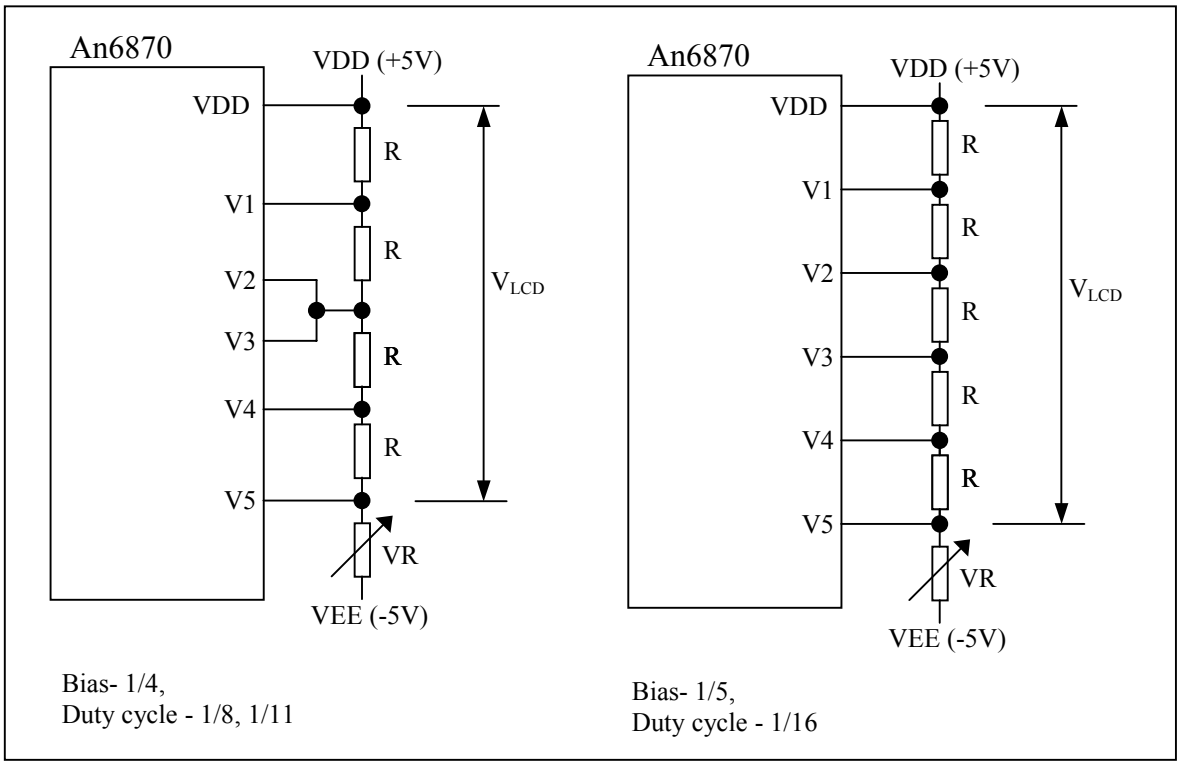


Figure 15. Drive Voltage Supply Example

4.5. Display Waveform Timing Diagram

Image contrast depends on display waveform characteristics – the shorter is duty cycle, the higher is contrast. Duty cycle is determined by the number of active COM-lines. For 1-line mode duty cycle is 1/8 or 1/11, for 2-line mode duty cycle is 1/16.

Contrast is also determined by V_{LCD} and bias voltages V1-V5. Use of a divider with 1/5 ratio allows to obtain higher contrast than with 1/4 ratio.

To increase durability of the LCD, output drivers must alternate polarity of LCD supply voltage periodically. For this purpose, the controller forms M signal. At that, two variants are possible:

- alternate V_{LCD} voltage polarity in each COM-line cycle. M state alternates two times in each COM cycle. M alternating frequency is equal to line frequency. This is "A" type of Display Waveform;
- alternate V_{LCD} voltage polarity in each frame cycle. M state alternates after full display update. M alternating frequency is equal to 1/2 of frame frequency. This is "B" type of Display Waveform.

The controller can use both types of Display Waveforms. The type is determined by controller mask option (see part 3.5, Appendix 1 and Appendix 2). Display Waveform type is chosen separately for Standard and Extended modes, any combination of types is allowed.

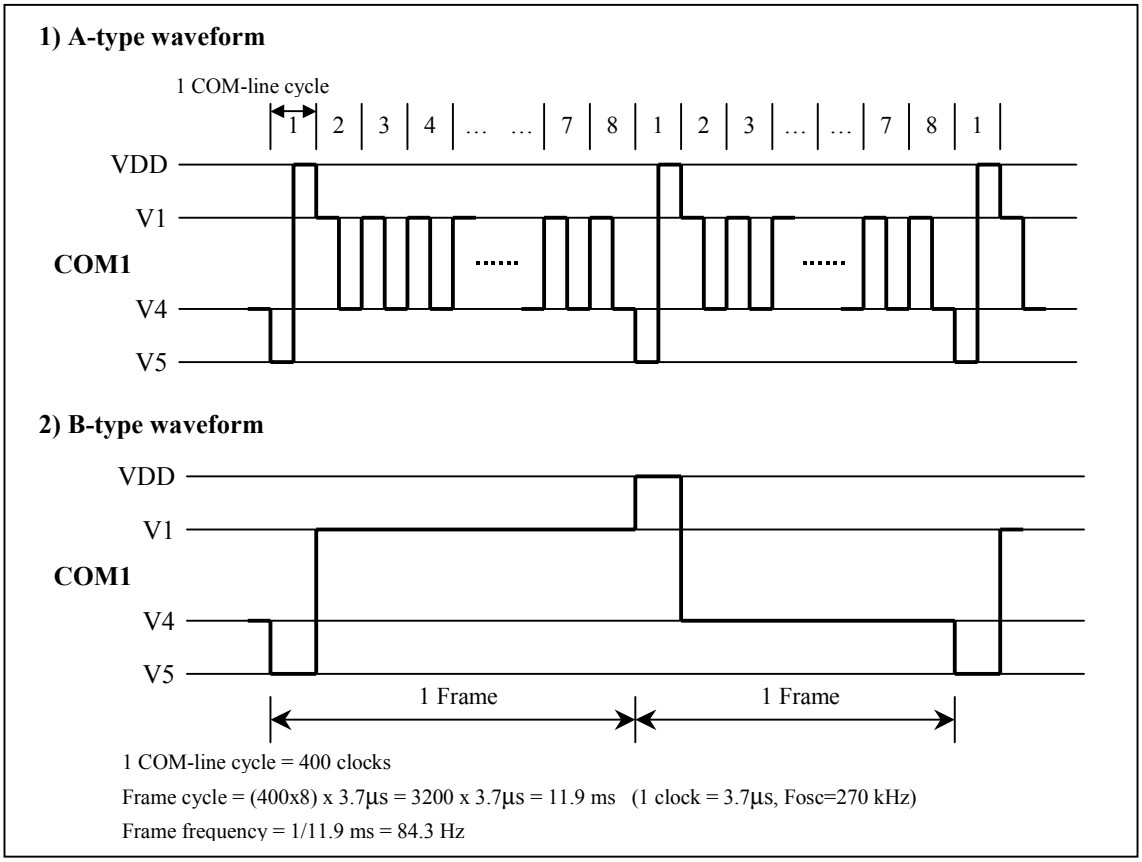


Figure 16. Timing diagram of Display Waveform for 1/8 duty cycle.

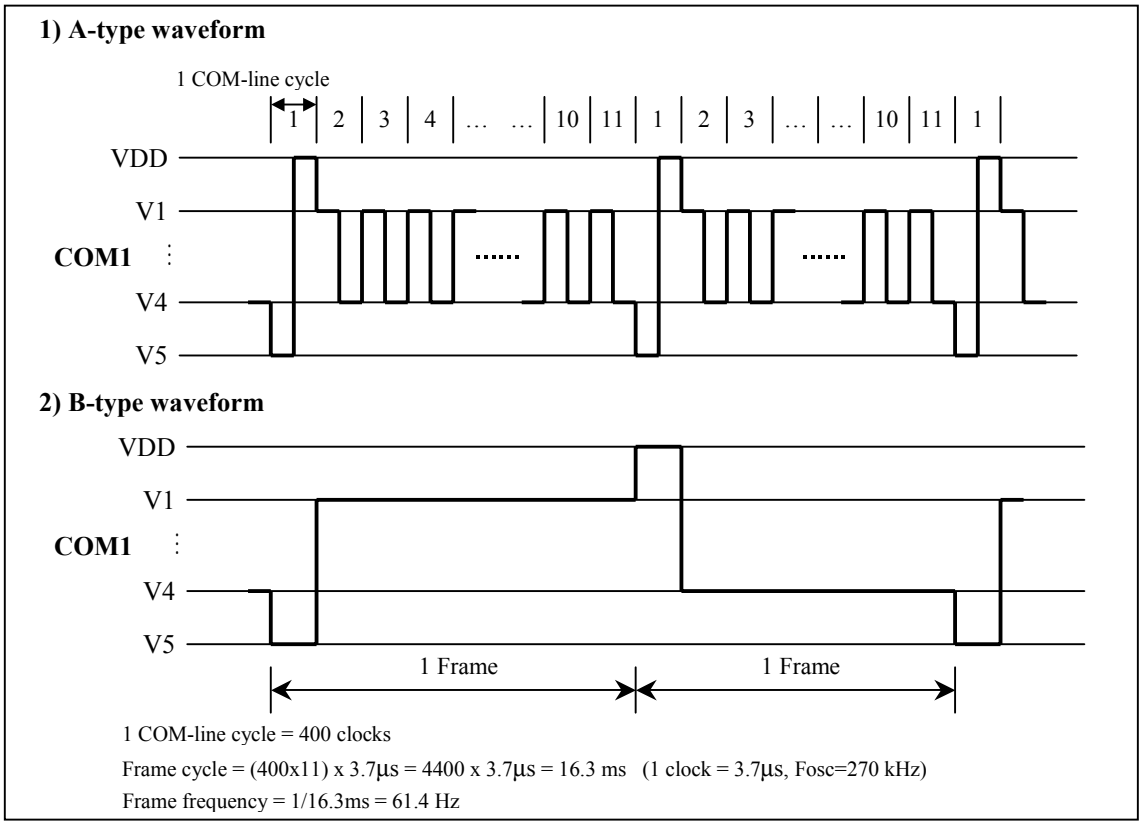


Figure 17. Timing diagram of Display Waveform for 1/11 duty cycle.

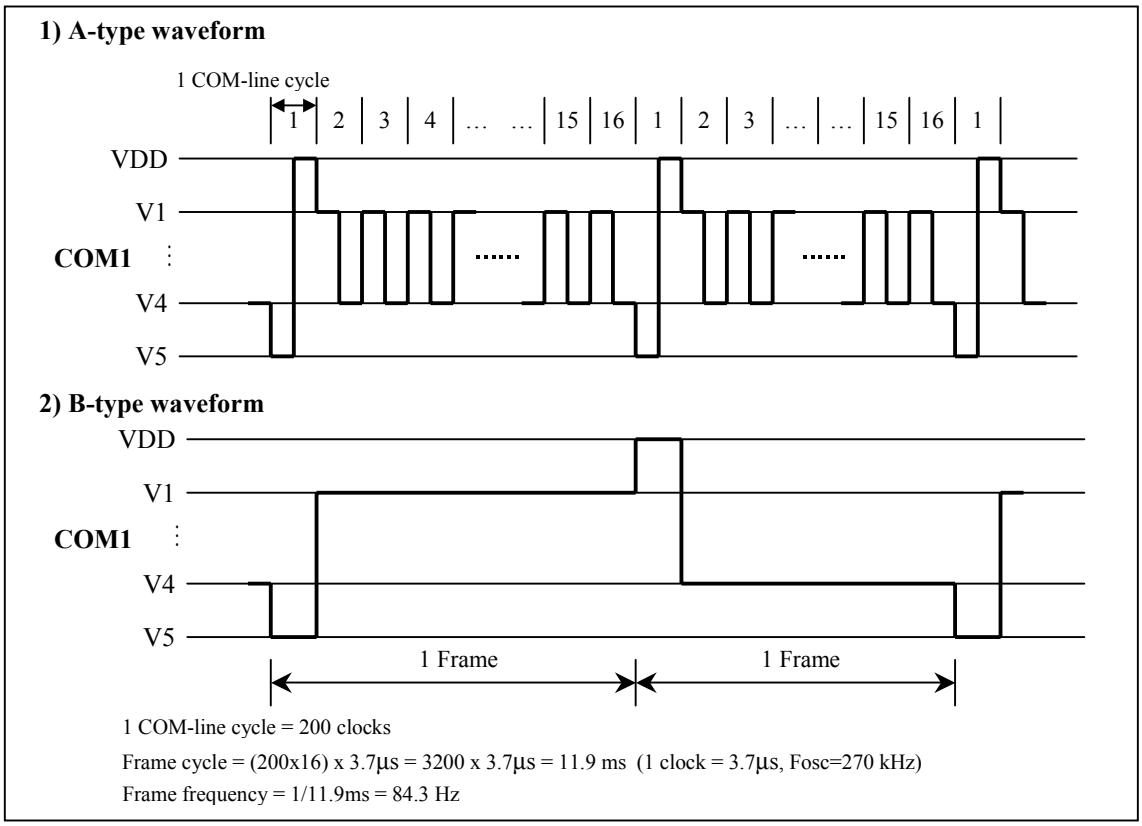


Figure 18. Timing diagram of Display Waveform for 1/16 duty cycle.

5. CONTROLLER PROGRAMMING

5.1. Initializing by instruction

Initializing by instruction in 8-bit interface mode

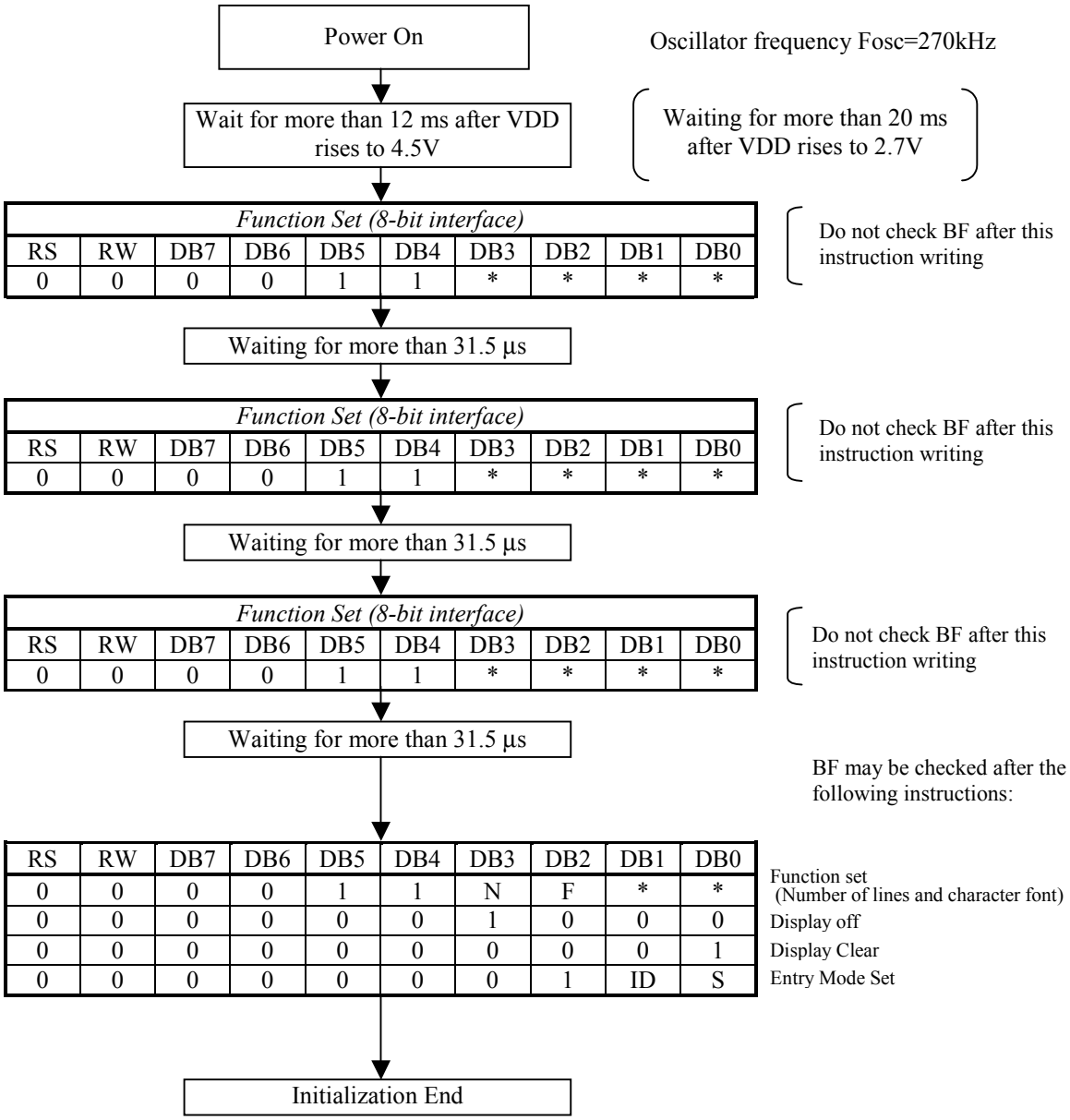


Figure 19. Initializing by instruction in 8-bit interface mode

Initializing by instruction in 4-bit interface mode

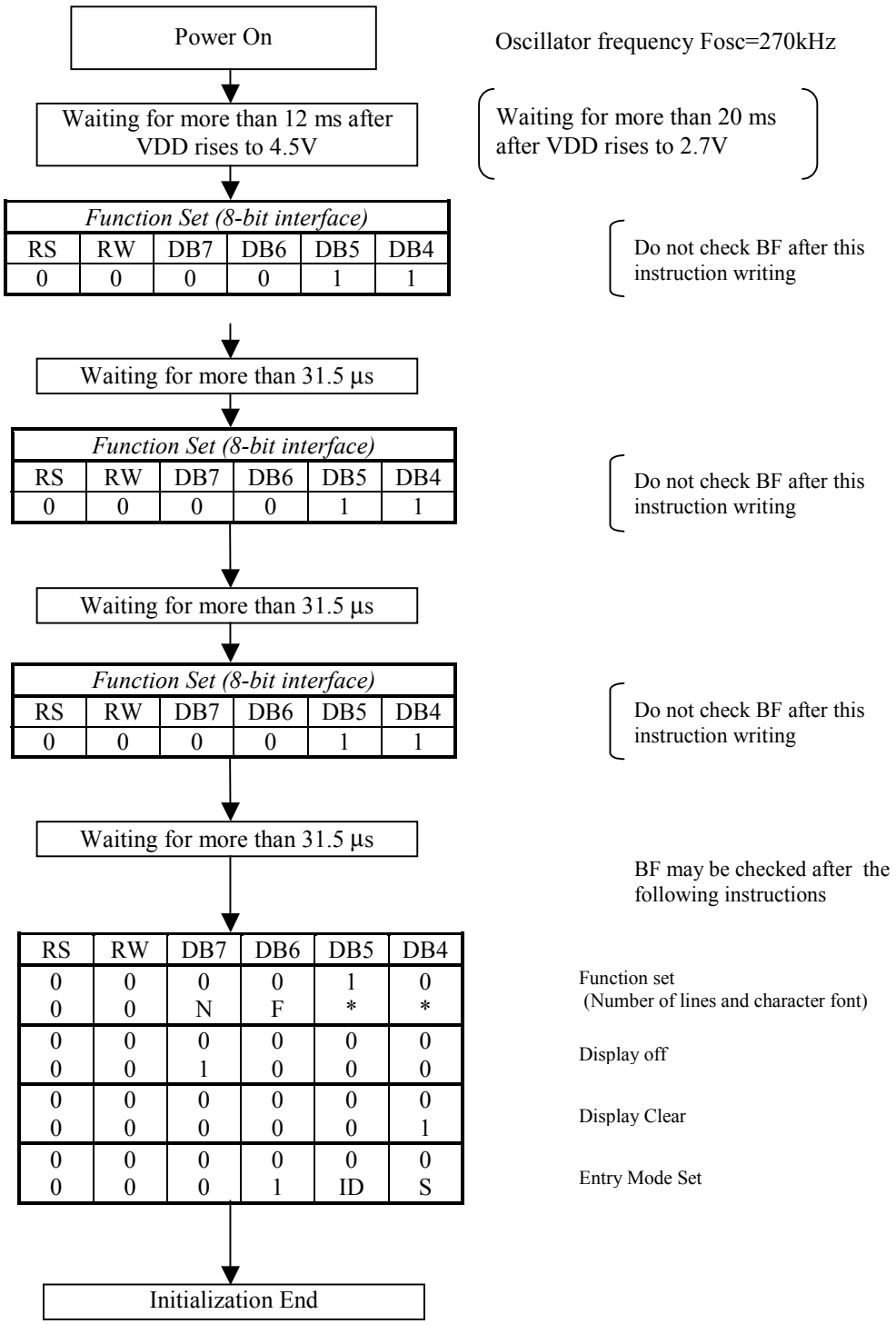


Figure 20. Initializing by instruction in 4-bit interface mode

5.2. Example of instruction and display correspondence in 8-bit interface mode

instruction sequence **LCD-panel**

1. Power Supply On: Initialized by the internal power on reset circuit

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	

2. Function Set: 8-bit, 2 lines, 5x8 font

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	1	1	0	*	*	

3. Display on, cursor on, blinking off

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	1	1	1	0	_

4. Entry Mode Set: address increment

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	1	1	0	_

5. Write Data to DDRAM: character A

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	1	0	0	0	0	0	1	**A_**

6. Write Data to DDRAM: character N

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	1	0	0	1	1	1	0	**AN_**

7. Write Data to DDRAM: character G

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	1	0	0	0	1	1	1	**ANG_**

8. Write Data to DDRAM: character S

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	1	0	1	0	0	1	1	**ANGS_**

9. Write Data to DDRAM: character T

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	1	0	1	0	1	0	0	**ANGST_**

10. Write Data to DDRAM: character R

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	1	0	1	0	0	1	0	**ANGSTR_**

11. Write Data to DDRAM: character E

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	1	0	0	0	1	0	1	**ANGSTRE_**

12. Write Data to DDRAM: character M

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	1	0	0	1	1	0	1	**ANGSTREM_**

13. Set DDRAM Address: 40h

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	1	1	0	0	0	0	0	0	**ANGSTREM** **_**

14. Write Data to DDRAM: character A

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	1	0	0	0	0	0	1	**ANGSTREM** **A_**

15. Write Data to DDRAM: character N

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	1	0

```
ANGSTREM
AN_
```

16. Write Data to DDRAM: character 6

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	1	1	0

```
ANGSTREM
AN6_
```

17. Write Data to DDRAM: character 8

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	1	0	0	0

```
ANGSTREM
AN68_
```

18. Write Data to DDRAM: character 7

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	1	1	1

```
ANGSTREM
AN687_
```

19. Write Data to DDRAM: character 0

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	0	0

```
ANGSTREM
An6870_
```

20. Write Data to DDRAM: character space

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	0	0	0	0	0

```
ANGSTREM
An6870 _
```

21. Entry Mode Set: Display Shift on during write

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	1

```
ANGSTREM
An6870 _
```

22. Write Data to DDRAM: character L

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	0	0

```
NGSTREM
N6870 L_
```

23. Write Data to DDRAM: character C

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	1	1

```
GSTREM
6870 LC_
```

24. Write Data to DDRAM: character M

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	0	1

```
STREM
870 LCM_
```

25. Cursor or Display Shift: cursor moves left

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	0	1	0	0	*	*

```
STREM
870 LCM
```

26. Write Data to DDRAM: character D

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	0	0

```
TREM
70 LCD_
```

27. Return Home

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	0

```
ANGSTREM
An6870 LCD
```

28. Display Clear

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

```
_
```

5.3. Example of instruction and display correspondence in 4-bit interface mode

Instruction sequence **LCD-panel**

1. Power Supply On: Initialized by the internal power on reset circuit

RS	RW	DB7	DB6	DB5	DB4

2. Function Set: 4-bit, 2 lines, 5x8 font

RS	RW	DB7	DB6	DB5	DB4
0	0	0	0	1	0
0	0	0	0	0	0

3. Display on, cursor on, blinking off

RS	RW	DB7	DB6	DB5	DB4
0	0	0	0	0	0
0	0	1	1	1	0

_

4. Entry Mode Set: address increment

RS	RW	DB7	DB6	DB5	DB4
0	0	0	0	0	0
0	0	0	1	1	0

_

5. Write Data to DDRAM: character A

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	0
1	0	0	0	0	1

A_

6. Write Data to DDRAM: character N

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	0
1	0	1	1	1	0

AN_

7. Write Data to DDRAM: character G

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	0
1	0	0	1	1	1

ANG_

8. Write Data to DDRAM: character S

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	1
1	0	0	0	1	1

ANGS_

9. Write Data to DDRAM: character T

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	1
1	0	0	1	0	0

ANGST_

10. Write Data to DDRAM: character R

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	1
1	0	0	0	1	0

ANGSTR_

Further instruction sequence is the same as in 8-bit interface mode (see part 5.2)

6. ELECTRICAL CHARACTERISTICS

6.1. Absolute Maximum Ratings

Parameter	Symbol	Unit	Value
Power supply voltage (1)	VDD	V	-0.3 to 7.0
Power supply voltage (2)	V_{LCD}	V	VDD-15 to VDD+0.3
Input voltage	V_{IN}	V	-0.3 to VDD+0.3

Note: VDD ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5.

6.2. Temperature Ratings

Parameter	Symbol	Unit	Value
Operating temperature	Topr	ºC	-30 to +85
Storage temperature	Tstg	ºC	-55 to +125

6.3. Power Supply Conditions Using Internal Reset Circuit

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VDD rise time	t_{rVDD}	4.5V at VDD=4.5V÷5.5V 2.7V at VDD=2.7V÷4.5V	0.1	-	20	ms
VDD off time	t_{OFF}	0.2V	1	-	-	

6.4. Electrical characteristics for VDD = 4.5V ÷ 5.5V

(VDD=4.5V ÷ 5.5V, Ta= -30 ÷ +85ºC)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Voltage	VDD	-	4.5	-	5.5	V
Supply Current	I_{DD}	RC-oscillator, external timing, VDD=5V, Fosc=270kHz, note 6.6.5	-	0.22	0.6	mA
Input Voltage (except OSC1)	V_{IH1}	-	2.2	-	VDD	V
	V_{IL1}	-	-0.3	-	0.6	
Input Voltage (OSC1)	V_{IH2}	-	VDD-1.0	-	VDD	
	V_{IL2}	-	-0.2	-	1.0	
Output Voltage (DB7-DB0)	V_{OH1}	I_{OH}= -0.205 mA	2.4	-	-	
	V_{OL1}	I_{OL}= 1.2 mA	-	-	0.4	
Output Voltage (except DB7-DB0)	V_{OH2}	I_{OH}= -40 µA	0.9 VDD	-	-	
	V_{OL2}	I_{OL}= 40 µA	-	-	0.1 VDD	
Voltage Drop on output drivers	Vd_{COM}	I_O= 0.1 mA, note 6.6.8	-	-	1	
	Vd_{SEG}		-	-	1	
Input Leakage Current	I_{IL}	V_{IN}= 0V ÷ VDD	-1	-	1	µA
Input Low Current RS, RW, DB0-DB7	I_{IN1}	V_{IN}= 0V, VDD=5V, (Pull-up to VDD), note 6.6.3	-40	-100	-180	
Input Low Current XMODE	I_{IN2}	V_{IN}= 0V, VDD=5V, (Pull-up to VDD), note 6.6.3	-6	-18	-50	
Internal Oscillator Frequency (with external resistor)	F_{IC}	Rf= 91KΩ ± 2%, VDD=5V, note 6.6.6	190	270	350	kHz
External Clock	F_{EC}	note 6.6.7	150	250	350	kHz
	duty		45	50	55	%
	rise time		-	-	0.2	µs
LCD Voltage	V_{LCD}	VDD-V5 (bias 1/5, 1/4)	4.6	-	10.0	V

Note: see part 6.6 "Electrical characteristics measurement conditions".

6.5. Electrical characteristics for VDD = 2.7V ÷ 4.5V

(VDD=2.7V ÷ 4.5V, Ta= -30 ÷ +85ºC)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Voltage	VDD	-	2.7	-	4.5	V
Supply Current	I_{DD}	RC-oscillator, external timing VDD=3V, Fosc=270kHz, note 6.6.5	-	0.13	0.3	mA
Input Voltage (except OSC1)	V_{IH1}	-	0.7 VDD	-	VDD	V
	V_{IL1}	-	-0.3	-	0.4	
Input Voltage (OSC1)	V_{IH2}	-	0.7 VDD	-	VDD	
	V_{IL2}	-	-	-	0.2 VDD	
Output Voltage (DB7-DB0)	V_{OH1}	I_{OH}= -0.1 mA	2.0	-	-	
	V_{OL1}	I_{OL}= 0.1 mA	-	-	0.4	
Output Voltage (except DB7-DB0)	V_{OH2}	I_{OH}= -40 µA	0.8 VDD	-	-	
	V_{OL2}	I_{OL}= 40 µA	-	-	0.2 VDD	
Voltage Drop on output drivers	Vd_{COM}	I_O= 0.1 mA, note 6.6.8	-	-	1	
	Vd_{SEG}		-	-	1.5	
Input Leakage Current	I_{IL}	V_{IN}= 0V ÷ VDD	-1	-	1	µA
Input Low Current RS, RW, DB0-DB7	I_{IN1}	V_{IN}= 0V, VDD=3V, (Pull-up to VDD), note 6.6.3	-10	-40	-90	
Input Low Current XMODE	I_{IN2}	V_{IN}= 0V, VDD=3V, (Pull-up to VDD), note 6.6.3	-1.5	-6	-15	
Internal Oscillator Frequency (with external resistor)	F_{IC}	Rf= 75 KΩ ± 2%, VDD=3V, note 6.6.6	190	270	350	kHz
External Clock	F_{EC}	note 6.6.7	150	250	350	kHz
	duty		45	50	55	%
	rise time		-	-	0.2	µs
LCD Voltage	V_{LCD}	VDD-V5 (bias 1/5, 1/4)	3.0	-	10.0	V

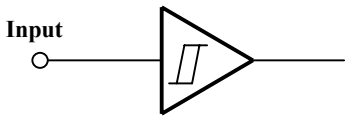
Note: see part 6.6 "Electrical characteristics measurement conditions".

6.6. Electrical characteristics measurement conditions

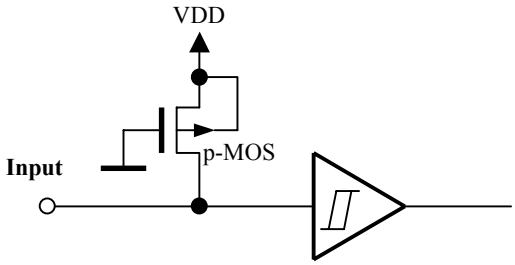
1) VDD≥V1≥V2≥V3≥V4≥V5.

2) Controller input/output pins circuit diagrams (except LCD output drivers):

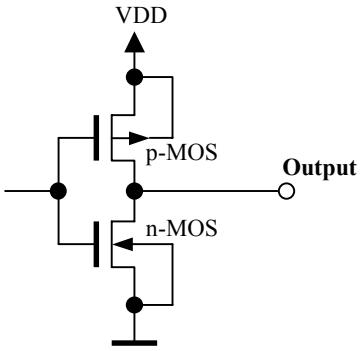
E pin (CMOS input without pull-up)



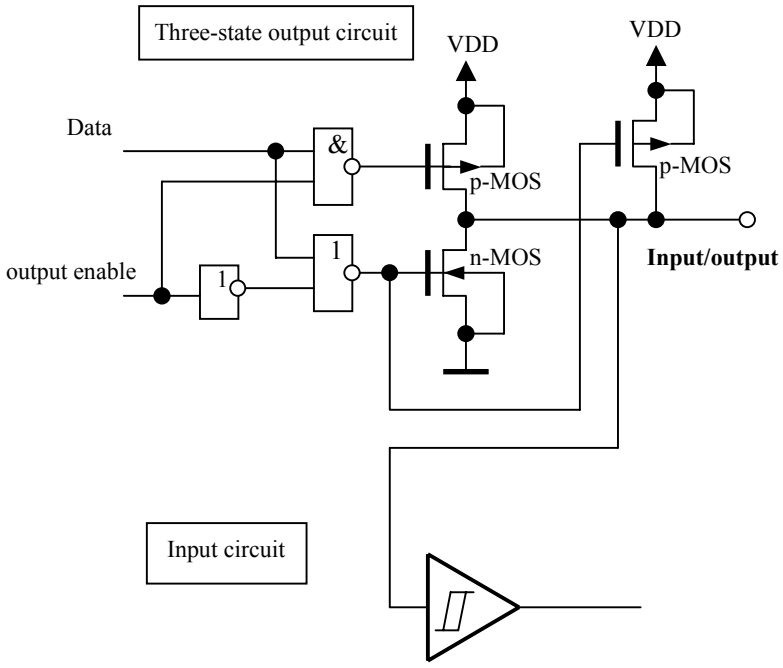
RS, RW pins (CMOS with pull-up)



CLK1, CLK2, D, M pins (CMOS output)



DB0-DB7 pins (CMOS input/output with pull-up)

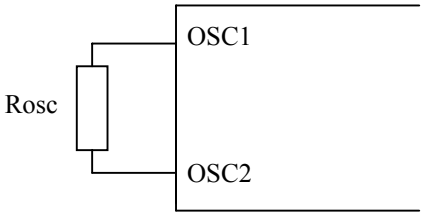


3) Pull-up current for input/output pins is measured only through pull-up transistor. Input/output current is excluded.

4) MPU interface input buffers use Schmitt trigger circuit with hysteretic not less than 0.15V (at VDD=5V).

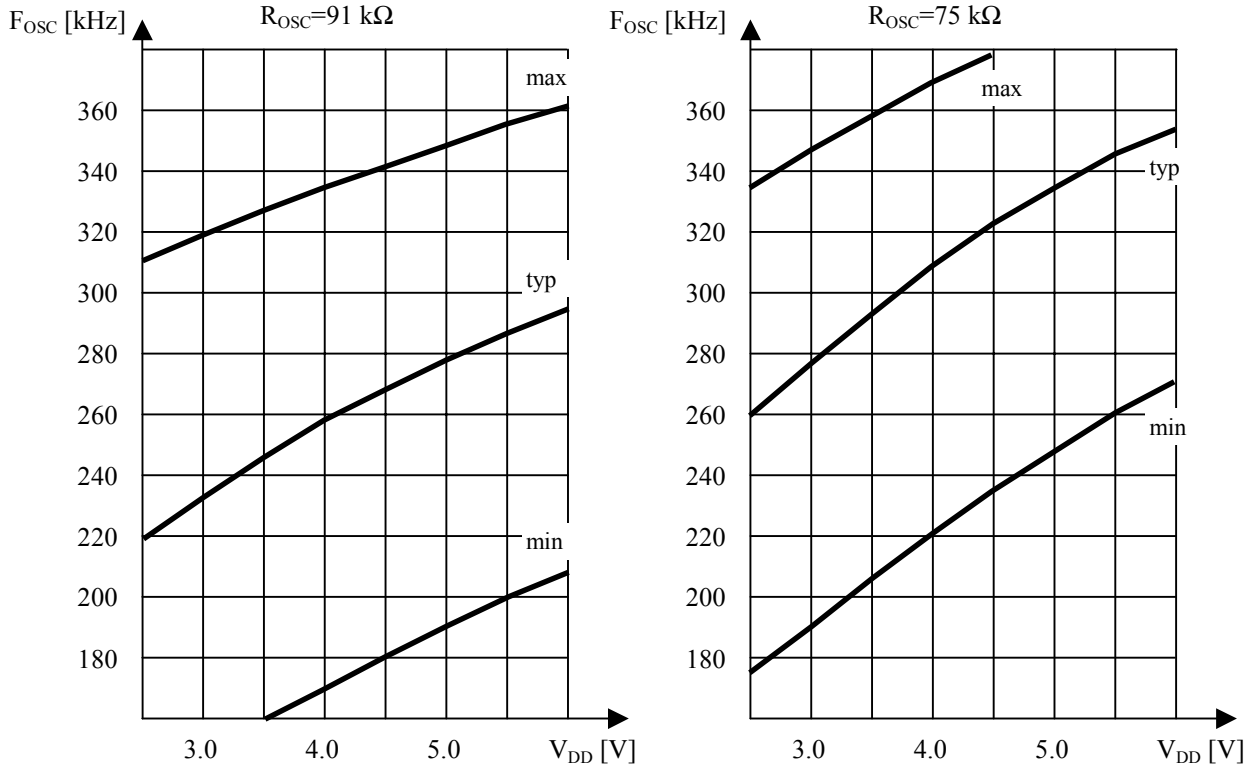
5) Consumption current does not include input/output currents. Consumption current is measured under the following conditions:
   - If intermediate levels are set for controller inputs, additional current from power supply flows through input buffer. To exclude this situation, input pins level must be fixed to GND or VDD;
   - Inputs and outputs with pull-up to VDD must have VDD level or be disconnected;
   - Resistive or capacitive output loads are absent.

6) External oscillator resistor connection:

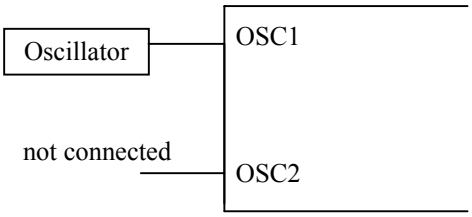


Rosc = 75 kΩ ±2% (at VDD=3V)
Rosc = 91 kΩ ±2% (at VDD=5V)

External capacitance at OSC1 influences the oscillator frequency. To decrease this influence, the length of pin wires for OCS1 and OSC2 must be minimal.

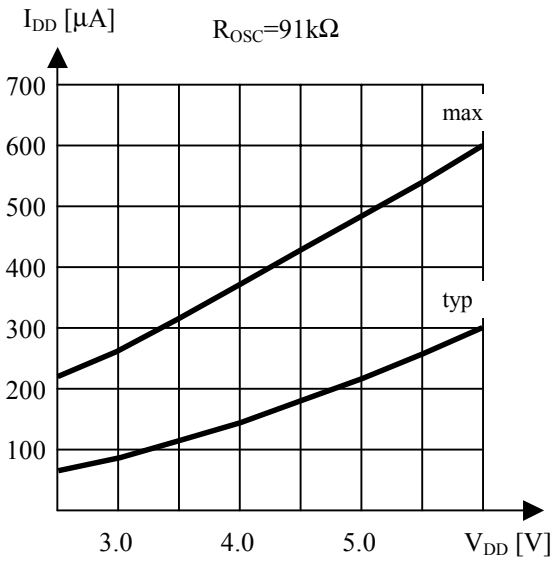


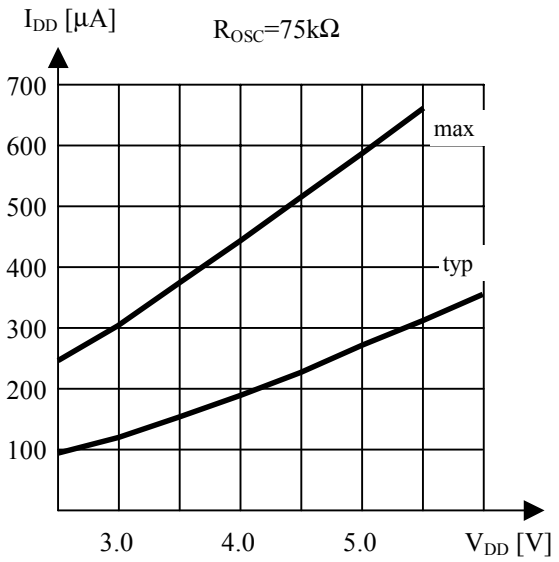
7) External oscillator connection:



8) COM and SEG outputs without load provide ±0.15V precision of output voltage relatively to V_{LCD} (VDD, V1, V2, V3, V4, V5).

9) The next diagrams show the consumption current vs. VDD dependence at R_{OSC} fixed. (Oscillator frequency variates according the VDD change - see part 6).





7. AC CHARACTERISTICS

7.1. VDD = 4.5V ÷ 5.5V

(VDD=4.5V ÷ 5.5V, Ta= -30 ÷ +85ºC)

Mode	Parameter	Symbol	Min	Max	Unit
Write Mode (Figure 21)	E Cycle Time	t_C	500		ns
	E Rise / Fall Time	t_r, t_f		25	
	E Pulse Width (High, Low)	t_W	220		
	RW and RS Setup Time	t_{SU1}	40		
	RW and RS Hold Time	t_{H1}	10		
	Data Setup Time	t_{SU2}	60		
	Data Hold Time	t_{H2}	10		
Read Mode (Figure 22)	E Cycle Time	t_C	500		ns
	E Rise / Fall Time	t_r, t_f		25	
	E Pulse Width (High, Low)	t_W	220		
	RW and RS Setup Time	t_{SU}	40		
	RW and RS Hold Time	t_H	10		
	Data Output Delay Time	t_D		120	
	Data Hold Time	t_{DH}	20		

7.2. VDD = 2.7V ÷ 4.5V

(VDD=2.7V ÷ 4.5V, Ta= -30 ÷ +85ºC)

Mode	Parameter	Symbol	Min	Max	Unit
Write Mode (Figure 21)	E Cycle Time	t_C	1000		ns
	E Rise / Fall Time	t_r, t_f		25	
	E Pulse Width (High, Low)	t_W	400		
	RW and RS Setup Time	t_{SU1}	60		
	RW and RS Hold Time	t_{H1}	20		
	Data Setup Time	t_{SU2}	140		
	Data Hold Time	t_{H2}	10		
Write Mode (Figure 22)	E Cycle Time	t_C	1000		ns
	E Rise / Fall Time	t_r, t_f		25	
	E Pulse Width (High, Low)	t_W	400		
	RW and RS Setup Time	t_{SU}	60		
	RW and RS Hold Time	t_H	20		
	Data Outpu Delay Time	t_D		360	
	Data Hold Time	t_{DH}	5		

7.3. Driver Interface Characteristics

Mode	Parameter	Symbol	Min	Max	Unit
Interface Mode with Extension Driver (Figure 23)	CLK1, CLK2 High Pulse Width	t_{WH}	800		ns
	CLK2 Low Pulse Width	t_{WL}	800		
	Clock Rise/Fall Time	t_r, t_f		100	
	CLK2 Setup Time	t_{SU1}	500		
	Data Setup Time	t_{SU2}	300		
	Data Hold Time	t_{DH}	300		
	M Delay Time	t_{DM}	-1000	1000	

7.4. Controller Interfaces Timing Diagrams

Write operation

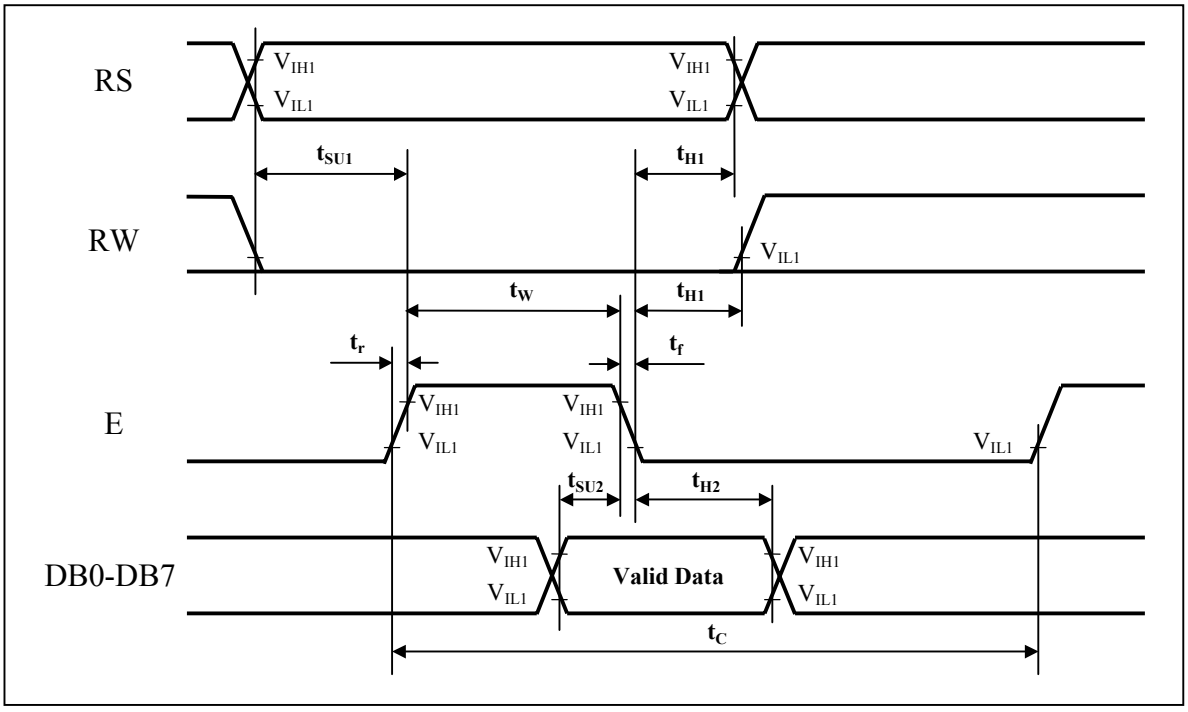


Figure 21. Write Mode Timing Diagram

Read operation

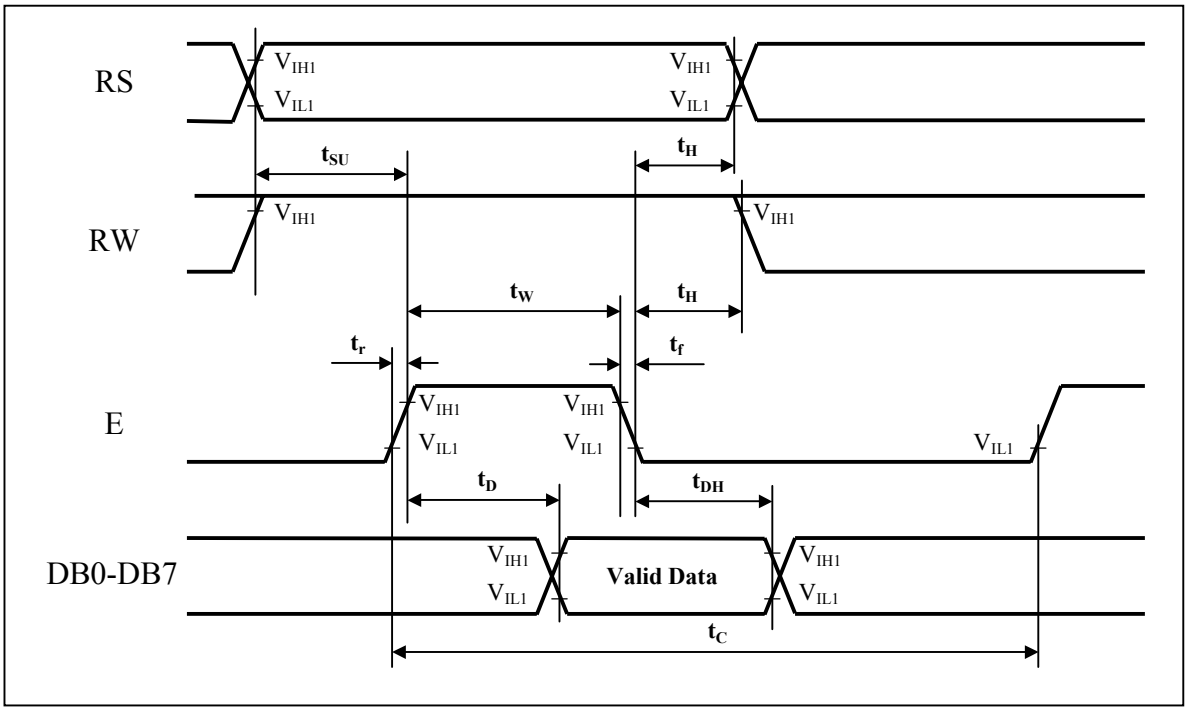


Figure 22. Read Mode Timing Diagram

Extension driver interface

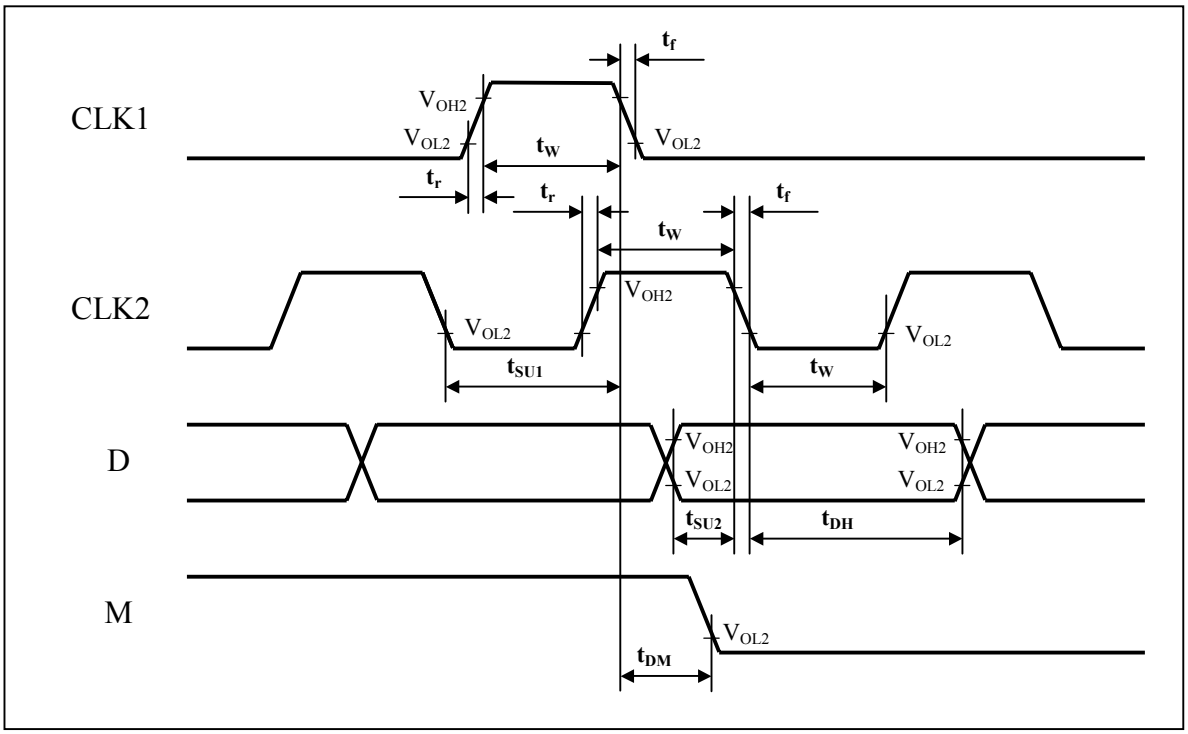


Figure 23. Extension Driver Interface Timing Diagram

8. APPLICATION INFORMATION

8.1. Application example of An6870 with extension drivers.

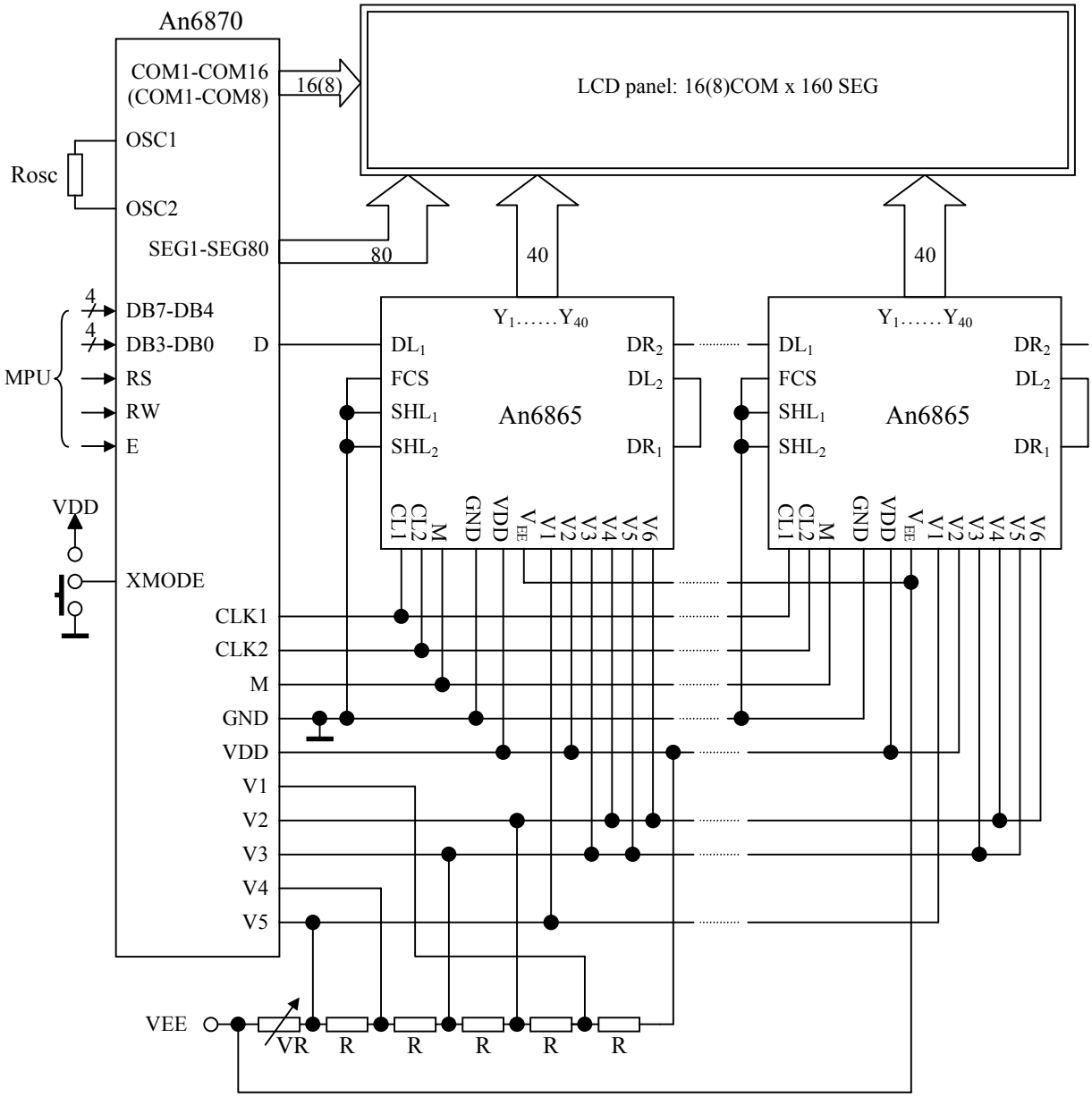


Figure 24. Application circuit of An6870.

8.2. Fast instruction executing mode

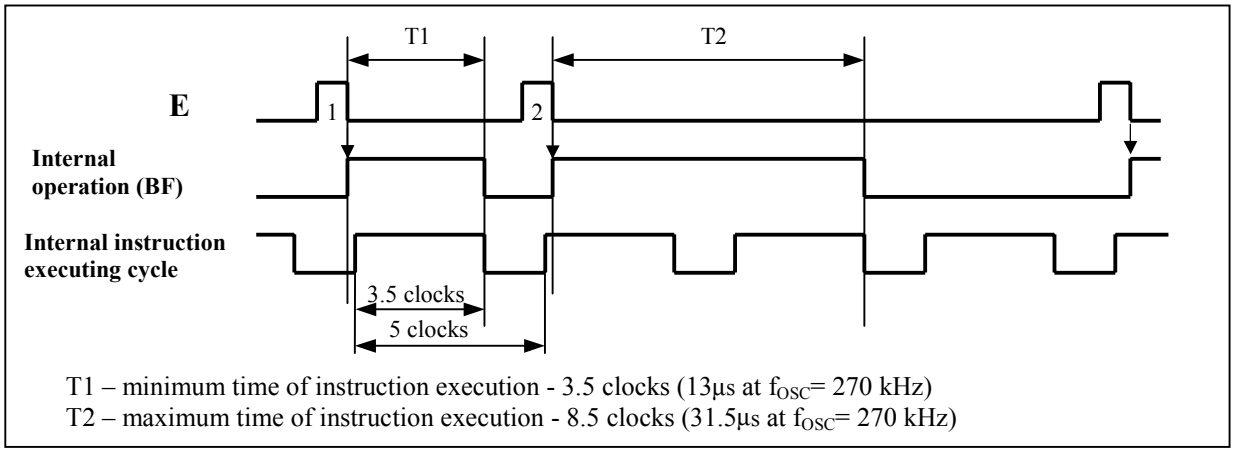
During the sequential execution of continuous instructions chain, there may be a situation, when every instruction will be executed in 5 clocks.

Figure 25 clarifies the conditions about different times of instruction executing. Instructions are executed during the appropriate phase 3.5 clocks long and 5 clocks period (see also part 2.6 "Timing Diagram"). Each instruction must pass one complete interval of the executing phase. Instruction executing begins at E fall and finishes at the end of the complete executing phase; BF has the same high level duration.

Figure 25 shows that instruction 1 is executed for approximately 3.5 clocks, because it is written directly before the executing phase. Instruction 2 comes after the beginning of the current executing phase, that is why it is executed for 5 clocks longer (approximately 8.5 clocks).

If MPU is capable to define the low level of BF and to write the next instruction during 1.5 clocks (5.5µs at f_{OSC}= 270kHz), which passes from the moment of completing of the previous phase of instruction executing till the beginning of the next one, then the instructions will be executed in every executing phase, i.e. at the highest speed when the sequential instruction writing. At that, writing and executing cycle for each instruction, beginning from the second one, will contain exactly 5 clocks (18.5µs at f_{OSC}= 270kHz).

Figure 26 shows one of the possible ways for fast instruction executing.



T1 – minimum time of instruction execution - 3.5 clocks (13µs at f_{OSC}= 270 kHz)
T2 – maximum time of instruction execution - 8.5 clocks (31.5µs at f_{OSC}= 270 kHz)

Figure 25. Instruction execution time

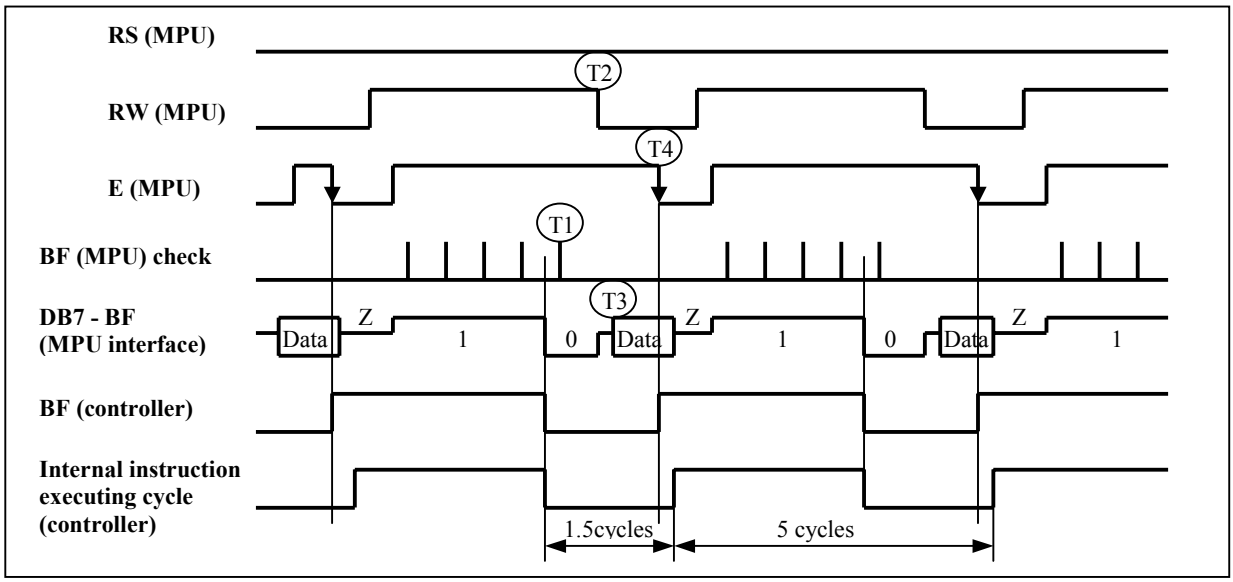


Figure 26. Example of fast instruction execution

After writing the instruction MPU releases DB bus, then sets Read BF and Address mode and high E level. Polling DB7 output, MPU waits till BF state becomes 0 (T1).

After that MPU switches to instruction write mode (T2), then it sets new data (T3) and writes the next instruction at E fall (T4). If MPU executes these operations during less than 1.5 clocks, then the new instruction will begin executing already in the next instruction executing phase, at that, duration of write and execute instruction period will be 5 clocks.

8.3. Sleep mode

The An6870 allows to use the sleep mode because the internal controller circuit has no floating nodes. All tri-states nodes have active pull-up to VDD in Z-state.

In the sleep mode the controller doesn't generate display waveform and doesn't accept instructions, but it keeps its state and memory content. Operation current in the sleep mode (I_{DD}) is significantly reduced (typical value is less then 15 μA).

To switch the controller to the sleep mode it is necessary to stop the oscillator and disconnect V1-V5 voltage divider from power supply. Before switching to the sleep mode, it is recommended to execute the Display Off instruction (see part 2.10) so that the controller wouldn't switch to the sleep mode during the memory access operation.

Switching to the sleep mode is made by hardware (see Figure 27). It's better to stop the oscillator at the OSC2 pin not to add parasitic capacity in OSC1 pin. It is not recommended to leave OSC1 pin open, because it has no active pull-up.

The simpliest way to stop oscillator is connecting OCS1 pin to GND or VDD. At this case additional current from power supply will flow through R_{OSC} (~55 μA at VDD=5V and R_{OSC}=91 kΩ).

V1-V5 divider resistors can be commutated both at VDD and VEE circuit.

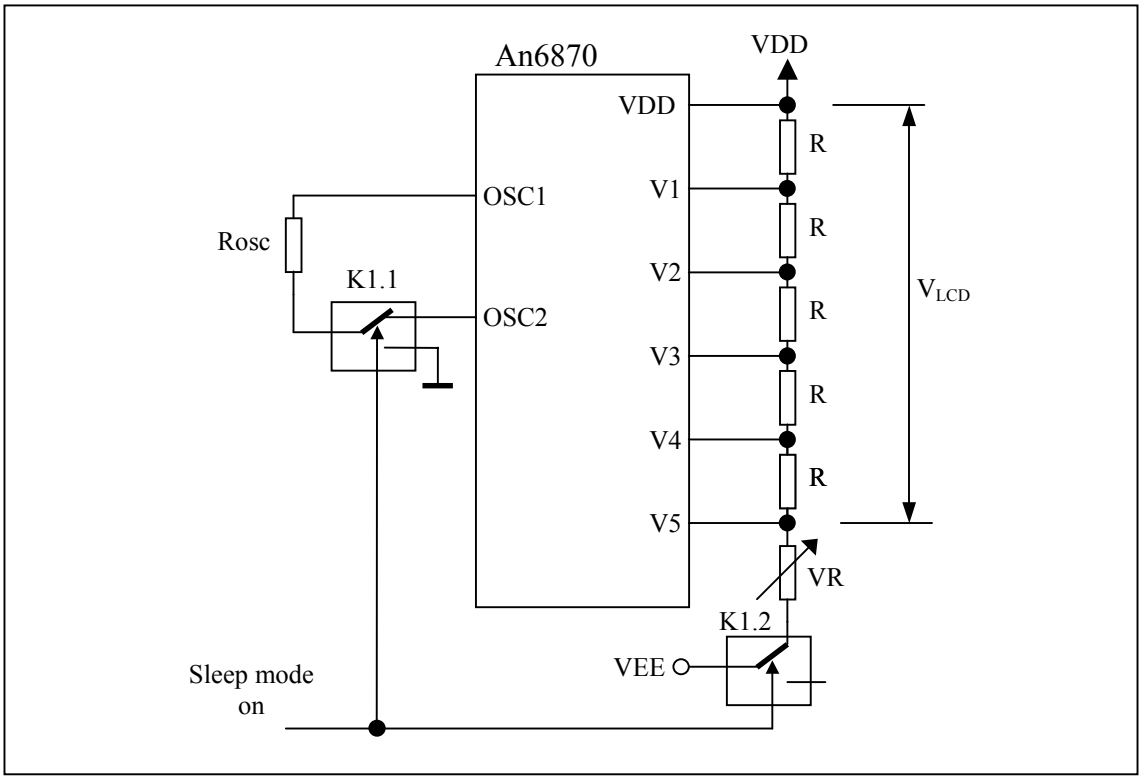


Figure 27. Sleep mode

8.4. Software estimation of oscillator frequency

Software estimation of oscillator frequency is based on evaluation of time interval between two events, depending from oscillator frequency.

It's possible to use BF and address reading procedure and any instruction that changes AC value.

Frequency determination is made the following way (see Figure 28):

MPU should write instruction that changes AC value (for example, Cursor Move). Then the controller is quickly switched into BF and address reading mode. It has minimum 1.5 cycles for this operation. Time interval T between moment of AC change and moment of BF resetting to 0 is exactly 2 clocks of oscillator timing diagram.

Oscillator frequency $\mathbf{F_{OSC} = 2/T.}$

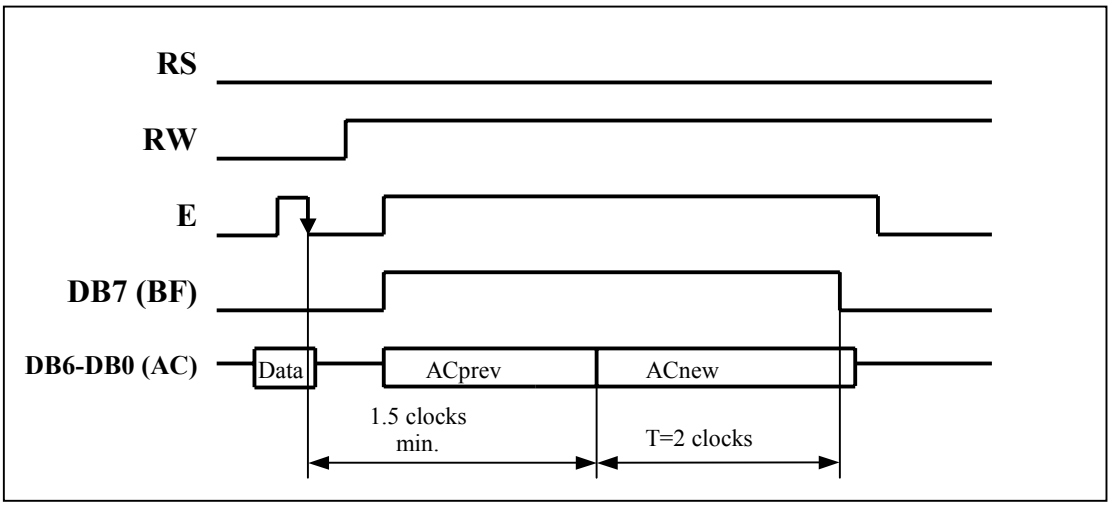


Figure 28. Software determination of oscillator frequency.

9. An6870A VERSION WITH THE LARGE FONT MODE

9.1. General information

The Large Font mode is special mask option of An6870A controller version with doubling character size horizontally and vertically. In this mode, characters have 10x15 dots size and can be displayed in one line up to 40 characters long.

Unique feature of this mode is operation with graphics-type LCD, because enlarged character pattern allows to leave spaces between them.

In this mode, it is also possible to display icons, for which there is a special COM-line. Totally 160 icons can be displayed (4 icons against each character pattern). Every icon can be switched on/off and set to blink or inverse blink mode. The second half of DDRAM is used as IconRAM.

There are 4 types of cursor: one-line cursor on COM15 or COM16 and two-line cursor on COM15-COM16 or COM14-COM15. Character or cursor blinking is also available.

The Large Font mode allows to get characters of the same quality as on the VGA computer display.

There are the following changes in the controller operating:

- DDRAM may contain 40 character codes and 40 bytes for icons control,
- CGRAM may contain 2 characters of 10x15 dot format or 20x15 bitmap,
- CGROM contains 126 characters of 10x15 dot format,
- AC operates in 2 independent ranges: from 0 to 39 and from 64 to 103,
- Function Set instruction bits determine Icons enabling, cursor position and cursor size selection,
- Display Clear instruction writes 20h code only to 40 bytes of DDRAM from 00h address.

9.2. DDRAM Addressing

All the DDRAM addresses are shared into two independent ranges. For the first range, AC has the following values: 0, 1, 2, … , 38, 39, 0, 1 , 2, … For the second range, AC has the following values: 64, 65, 66, … , 102, 103, 64, 65, 66, …

Address range is selected by Set DDRAM Address instruction.

For the first address range, DDRAM contains 40 character codes, and for the second address range, DDRAM contains 40 bytes for icons control (see Figure 29).

9.3. Icon displaying

Each byte of DDRAM in 40h-67h address range controls 4 icons against one character pattern. Each icon is controlled by 2 bits, which determinate icon visibility according to normal and inverse blinking phase (see Tables 14 and 15). Icons are displayed at 3, 5, 7 and 9 SEG outputs against each character pattern (see Figures 33-35).

Icons display position is stable, i.e. each icon corresponds to strictly determined DDRAM bits. It means that display shift doesn’t influence icons displaying (see Figure 30).

Normal and inverse icons blinking allows to display different dynamic effects without additional MPU loading. Another example of icons use is creating of overline and underline elements for different national characters.

Table 14. Icon control bits description

Displaying at normal blinking phase	Displaying at inverse blinking phase	Icon order (SEG outputs per each icon)
D7	D6	First icon (SEG3)
D5	D4	Second icon (SEG5)
D3	D2	Third icon (SEG7)
D1	D0	Fourth icon (SEG9)

Table 15. Icon control bits state

Dn+1 Dn	State
00	Off
01	Syncronous icon blinking with cursor or character blinking
10	Inverse icon blinking
11	On

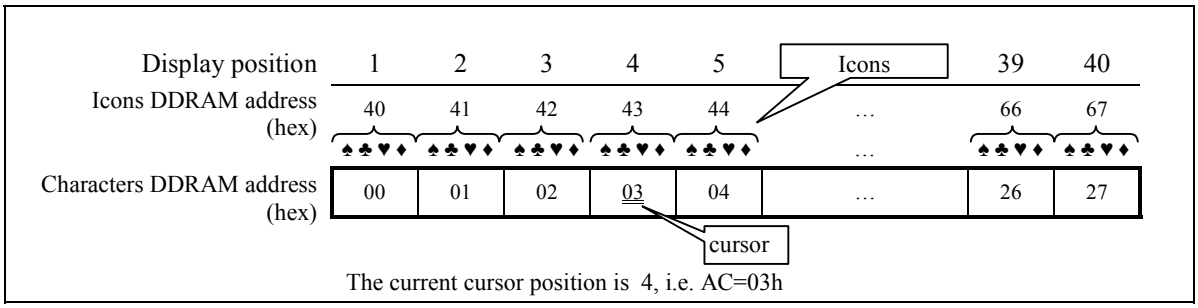


Figure 29. Display in the Large Font mode without shifting

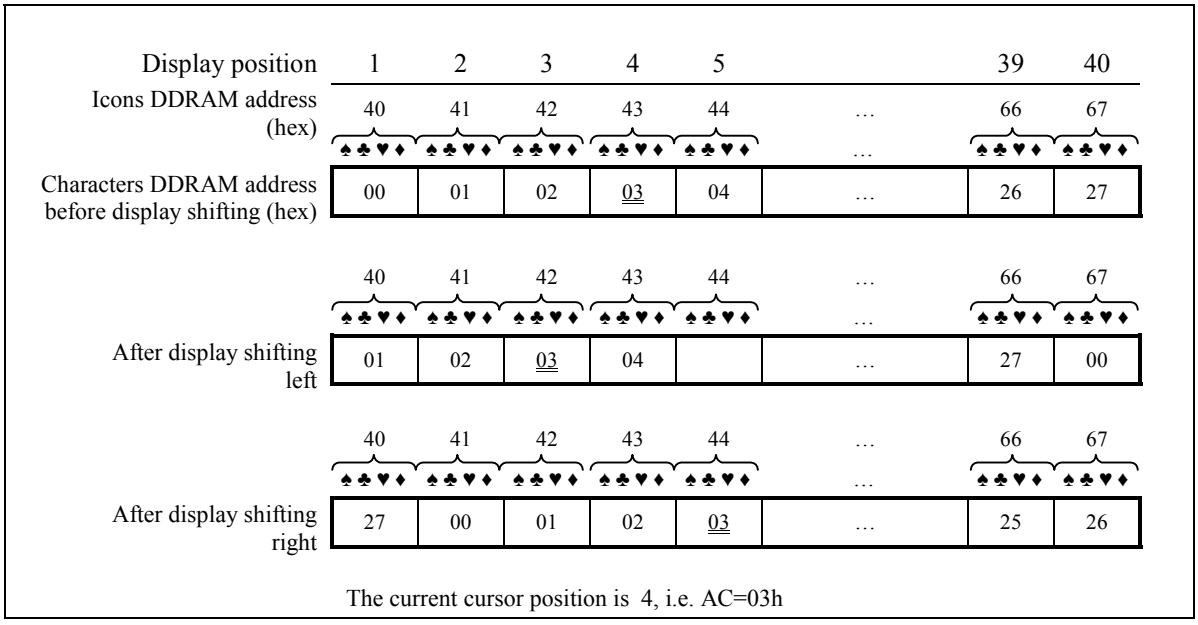


Figure 30. Display shifting in the Large Font mode

9.4. Display Waveform in the Large Font mode

The controller operates in the Large Font mode like in standard 2-line mode with the only difference: total number of SEG outputs may reach 400 (10 SEG for each of 40 characters), which is two times more than in standard mode (see part 2.6).

When increasing quantity of displayed information may result in decreasing of display refresh frequency down to 40 Hz at Fosc=270 kHz ± 30%. To enlarge it up to ≈60 Hz it is recommended to increase Fosc up to 400 kHz.

9.5. Instruction execution

When increasing oscillator frequency, instruction execution time decreases. All instructions, except Display Clear, are executed during not more than 8.5 clocks. At Fosc=400 kHz instruction execution time is equal to 8.5x2.5µs =21.25µs.

Display Clear instruction is executed during not more than 203.5 clocks. Executing time for this instruction is 203.5x2.5µs =508.75µs.

9.6. Changes in Instruction Set

Display Clear

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Display Clear instruction writes 20h to 0-27h DDRAM addresses. Then AC and start address counter set to 0. The DDRAM content at 40h-67h addresses doesn't change. I/D bit of Entry Mode Set instruction sets to 1, S bit state doesn't change.

Function Set

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	IE	CP	CS	I

This instruction is used to setup basic controller modes.

DL: Sets the interface data bus width. Bus width is 8-bit (DB7-DB0) when DL=1, and 4-bit (DB7-DB4) when DL=0. When 4-bit width is selected, data must be transferred in two passes.

IE: Icons displaying enabling (1 is On, 0 is Off).

CP: Sets cursor position (see Table 16).

CS: Sets cursor size (see Table 16).

Table 16. Cursor size and position

CP	CS	Cursor size and position
0	0	1-line cursor at COM15
0	1	2-line cursor at COM14 - COM15
1	0	1-line cursor at COM16
1	1	2-line cursor at COM15 - COM16

I: Display inversion (see part 2.10).

9.7. CGROM coding

CGROM contains 126 characters of 10x15 dot format in code range 02h-7Fh. D7 (high order bit) is not used and reserved for further developments (see Table 17).

Characters of any format (limited to 10x15) may be coded into CGROM (for example, 8x14, 7x12 dots). Empty COM and SEG outputs may be used for spaces between characters or they may be left unconnected.

Table 17. CGROM addressing in the Large Font mode

Character code							COM[1..16]				Data										
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0=0					A_0=1					
											MSB				LSB	MSB				LSB	
											Q_4	Q_3	Q_2	Q_1	Q_0	Q_4	Q_3	Q_2	Q_1	Q_0	
0	1	1	0	0	0	1	0	0	0	0	*	*	*	*	*	*	*	*	*	*	Icon line
							0	0	0	1	0	0	0	0	0	0	0	0	0	0	
							0	0	1	0	0	0	0	0	0	0	0	0	0	0	
							0	0	1	1	0	0	0	0	0	0	0	0	0	0	
							0	1	0	0	0	0	0	0	0	0	0	0	0	0	
							0	1	0	1	0	0	**1**	**1**	**1**	**1**	**1**	0	0	0	
							0	1	1	0	0	0	0	0	0	0	**1**	**1**	0	0	
							0	1	1	1	0	0	**1**	**1**	**1**	**1**	**1**	**1**	0	0	**Character**
							1	0	0	0	0	**1**	**1**	0	0	0	**1**	**1**	0	0	
							1	0	0	1	0	**1**	**1**	0	0	0	**1**	**1**	0	0	
							1	0	1	0	0	**1**	**1**	0	0	0	**1**	**1**	0	0	
							1	0	1	1	0	0	**1**	**1**	**1**	**1**	0	**1**	**1**	0	
							1	1	0	0	0	0	0	0	0	0	0	0	0	0	
							1	1	0	1	0	0	0	0	0	0	0	0	0	0	cursor position
							1	1	1	0	0	0	0	0	0	0	0	0	0	0	
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	
0	0	0	0	0	1	1	0	0	0	0	*	*	*	*	*	*	*	*	*	*	Icon line
							0	0	0	1	0	0	0	0	0	0	0	0	0	0	
							0	0	1	0	0	0	0	0	0	0	0	0	0	0	
							0	0	1	1	0	0	0	0	0	0	0	0	0	0	
							0	1	0	0	0	0	**1**	**1**	**1**	**1**	**1**	0	0	0	
							0	1	0	1	0	**1**	**1**	0	0	0	**1**	**1**	0	0	
							0	1	1	0	0	**1**	**1**	0	0	0	**1**	**1**	0	0	
							0	1	1	1	0	**1**	**1**	0	**1**	**1**	**1**	0	0	0	**Character**
							1	0	0	0	0	**1**	**1**	0	0	0	**1**	**1**	0	0	
							1	0	0	1	0	**1**	**1**	0	0	0	**1**	**1**	0	0	
							1	0	1	0	0	**1**	**1**	**1**	0	0	**1**	**1**	0	0	
							1	0	1	1	0	**1**	**1**	0	**1**	**1**	**1**	0	0	0	
							1	1	0	0	0	**1**	**1**	0	0	0	0	0	0	0	
							1	1	0	1	0	**1**	**1**	0	0	0	0	0	0	0	cursor position
							1	1	1	0	0	**1**	**1**	0	0	0	0	0	0	0	
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	

Notes:
1. 7-bit character code, corresponding with address A_{11}-A_5, is read from DDRAM (D6-D0) according to character position on display. D7 state has no effect.
2. Addresses A_4-A_1 – COM[1..16]-line number.
3. Address A_0 distinguishes between two parts of 10x15 character, defined by data order at display refresh.
4. Pixel is "on" corresponding to "1" in CGROM.

9.8. Character pattern writing into CGRAM

Two large character patterns with codes 00h and 01h may be written to CGRAM (see Table 18). D7-D5 bits are not used and may contain any information.

Table 18. CGRAM addressing in the Large Font mode

CGRAM selection sign							CGRAM Address				Data										
Character code							COM[1..16]														
						AC_5	AC_3	AC_2	AC_1	AC_0	AC_4=0					AC_4=1					
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0=0					A_0=1					
											MSB				LSB	MSB				LSB	
											Q_4	Q_3	Q_2	Q_1	Q_0	Q_4	Q_3	Q_2	Q_1	Q_0	
0	0	0	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*	*	*	Icon line
							0	0	0	1	0	0	0	0	0	0	0	0	0	0	
							0	0	1	0	0	1	1	1	1	1	1	1	1	0	
							0	0	1	1	0	0	0	0	0	0	0	0	0	0	
							0	1	0	0	0	0	0	0	0	0	0	0	0	0	
							0	1	0	1	0	0	1	1	1	1	1	0	0	0	
							0	1	1	0	0	0	0	0	0	0	1	1	0	0	
							0	1	1	1	0	0	1	1	1	1	1	1	0	0	**First**
							1	0	0	0	0	1	1	0	0	0	1	1	0	0	**character**
							1	0	0	1	0	1	1	0	0	0	1	1	0	0	
							1	0	1	0	0	1	1	0	0	0	1	1	0	0	
							1	0	1	1	0	0	1	1	1	1	0	1	1	0	
							1	1	0	0	0	0	0	0	0	0	0	0	0	0	
							1	1	0	1	0	0	0	0	0	0	0	0	0	0	Cursor position
							1	1	1	0	0	0	0	0	0	0	0	0	0	0	
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	
0	0	0	0	0	0	1	0	0	0	0	*	*	*	*	*	*	*	*	*	*	Icon line
							0	0	0	1	0	0	0	0	0	0	0	0	0	0	
							0	0	1	0	0	1	1	1	1	1	1	1	0	0	
							0	0	1	1	0	0	0	0	0	0	0	0	0	0	
							0	1	0	0	0	0	1	1	1	1	1	0	0	0	
							0	1	0	1	0	1	1	0	0	0	1	1	0	0	
							0	1	1	0	0	1	1	0	0	0	1	1	0	0	
							0	1	1	1	0	1	1	0	1	1	1	0	0	0	**Second**
							1	0	0	0	0	1	1	0	0	0	1	1	0	0	**character**
							1	0	0	1	0	1	1	0	0	0	1	1	0	0	
							1	0	1	0	0	1	1	1	0	0	1	1	0	0	
							1	0	1	1	0	1	1	0	1	1	1	0	0	0	
							1	1	0	0	0	1	1	0	0	0	0	0	0	0	
							1	1	0	1	0	1	1	0	0	0	0	0	0	0	Cursor position
							1	1	1	0	0	1	1	0	0	0	0	0	0	0	
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	

Notes:
1. 7-bit character code, corresponding with address A_{11}-A_5, is read from DDRAM (D6-D0) according to character position on display.
2. Addresses A_{11}-A_6 of CGRAM are indicating selection of CGRAM (A_{11}-A_6=00000).
3. Address A_5 – CGRAM character code (2 characters 10x15 at all).
4. Addresses A_4-A_1 – COM[1..16]-line number.
5. Address A_0 distinguishes between two parts of 10x15 character, defined by display waveform type.
6. AC_5-AC_0 – address counter (AC) bits while read/write data.
7. CGRAM Q_7-Q_5 bits are not displayed and can be used as conventional memory.
8. Pixel is "on" corresponding to "1" in CGROM.

9.9. CMID coding

In the Large Font mode some CMID bit functions are differents from the standard mode (see Table 19). The controller version identification in 4 high order CMID bytes is not changed. LF bit is 1 indicates the Large Font mode.

Table 19. CMID bits in the Large Font mode

Address		Identification code of An6870A								Parameter
Dec.	Hex.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
120	78h	0	1	0	0	0	0	0	1	An6870 Chip Identifier
121	79h	0	1	0	0	1	1	1	0	
122	7Ah	0	1	0	0	0	1	0	0	
123	7Bh	0	1	0	0	0	1	1	0	
124	7Ch	0	V	V	V	V	V	V	V	CGROM version
125	7Dh	IER	IEF	CPR	CPF	CSR	CSF	IN	IX	Configuration
126	7Eh	LF	SZ	CBN	CBX	WFN	WFX	CS	I	Config./Current state
127	7Fh	X	IE	CP	D	C	B	ID	S	Current state

Permanent part

V	CGROM version
IER	Initial state of Icon displaying enable bit
IEF	1 – Icon display enable fix IE state, 0 – Init IE state when power on (software controllable)
CPR	Initial cursor position bit
CPF	1 – Cursor position bit fix, 0 –Init CP state when power on (software controllable)
CSR	Initial cursor size bit
CSF	1 – Cursor size bit fixing, 0 –Init CS state when power on (software controllable)
IN	Inverse enable when XMODE=1
IX	Inverse enable when XMODE=0
LF	Large Font mode (1 – for version An6870A)
SZ	CGROM Size: 1 for double size (for further development)
CBN	Cursor Blink when XMODE=1
CBX	Cursor Blink when XMODE=0
WFN	WaveForm type when XMODE=1 (0- A-type, 1- B-type)
WFX	WaveForm type when XMODE=0 (0- A-type, 1- B-type)

Variable part

CS	Cursor size	D	Display on
I	Current inversion mode	C	Cursor on
X	XMODE status	B	Blinking on
IE	Icons display enable	ID	Inc. or dec. of address when reading/writing data
CP	Cursor position	S	Display shift enable when writing to DDRAM

9.10. Controller initialization in the Large Font mode

An internal reset circuit automatically initializes the An6870A when the power is turned on. Initialization procedure performs the following functions:

- Display Clear writes 20h into all character DDRAM addresses, zero values are also written into Icon memory;
- Function Set:
  DL=1, 8-bit interface *),
  IE=0, Icons are off *),
  CP=0, CS=0, cursor at COM15 *);
  I=0, display inversion is off if software inversion control is enabled;
- Display On/Off:
  D=0, display is off,
  C=0, cursor is off,
  B=0, blinking is off;
- Entry Mode Set:
  I/D=1, address increment mode when data reading/writing,
  S=0, disable display shift when data writing.

*) DL, IE, CP, CS bits state of Function Set instruction can be defined by the Customer at new mask option order (see part 3.5. "Controller mask option").

If electrical characteristics do not satisfy conditions in part 6.3 "Power Supply Conditions Using Internal Reset Circuit", or VDD voltage influence occurs, reset procedure may not function properly and initialization error will occur. In this case initialization by instruction may be performed (see Figure 31 and Figure 32).

9.11. Display information features in the Large Font mode

The An6870A in the Large Font mode can display characters on graphics-type LCD. 10x15 dot character format allows to leave blank columns (al least 1 SEG-line) and rows (1 or 2 COM-lines) between characters. There are different LCD panel formats possible: from 14 to 16 rows for 1-line and from 30 to 32 rows for 2-line mode (see Figure 33 and 35). Display length is limited up to 40 characters.

Graphics-type LCD allows to display 20x15 dot bitmap, combined from two CGRAM cells. Bitmap information is written to CGRAM according to Table 18. Codes 00h and 01h are written into desired display position and bitmap is displayed on LCD.

There are many ways to display information on text-type LCD. These variants are limited only by maximum character size (10x15). It is necessary to mean, that the character format on the LCD should correspond to the size of the CGROM characters. The Customer Order filling procedure is given in part 3.6. The example of LCD connection display 8x14 dot characters is shown in Figure 34.

9.12. Changes in electrical characteristics

In the Large Font mode with Fosc = 400 kHz typical value of consumption current I_{DD} is increased by 1.5 times.

9.13. Initializing by instruction in 8-bit interface mode

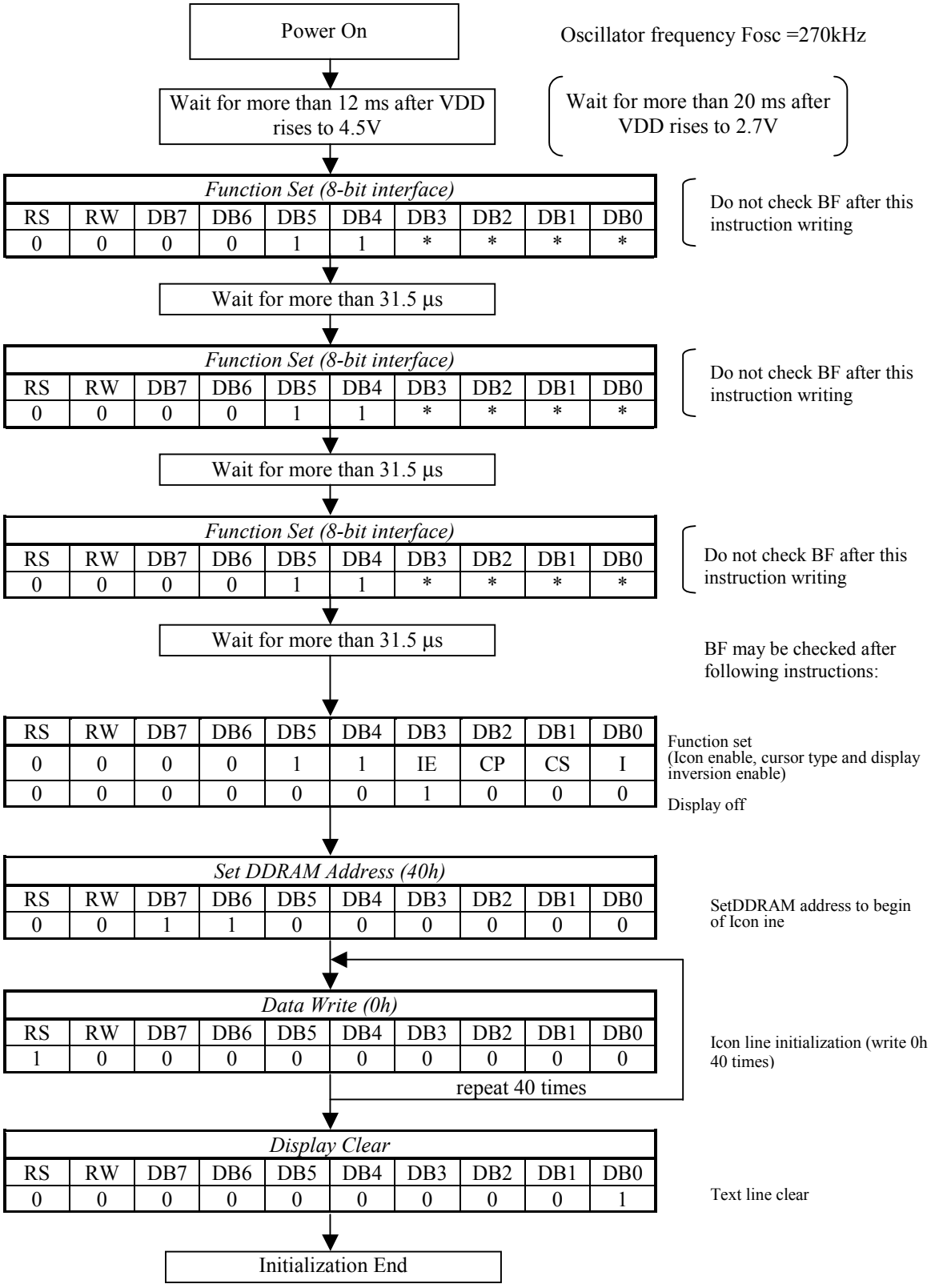


Figure 31. Initializing by instruction in the Large Font and 8-bit interface mode.

9.14. Initializing by instruction in 4-bit interface mode

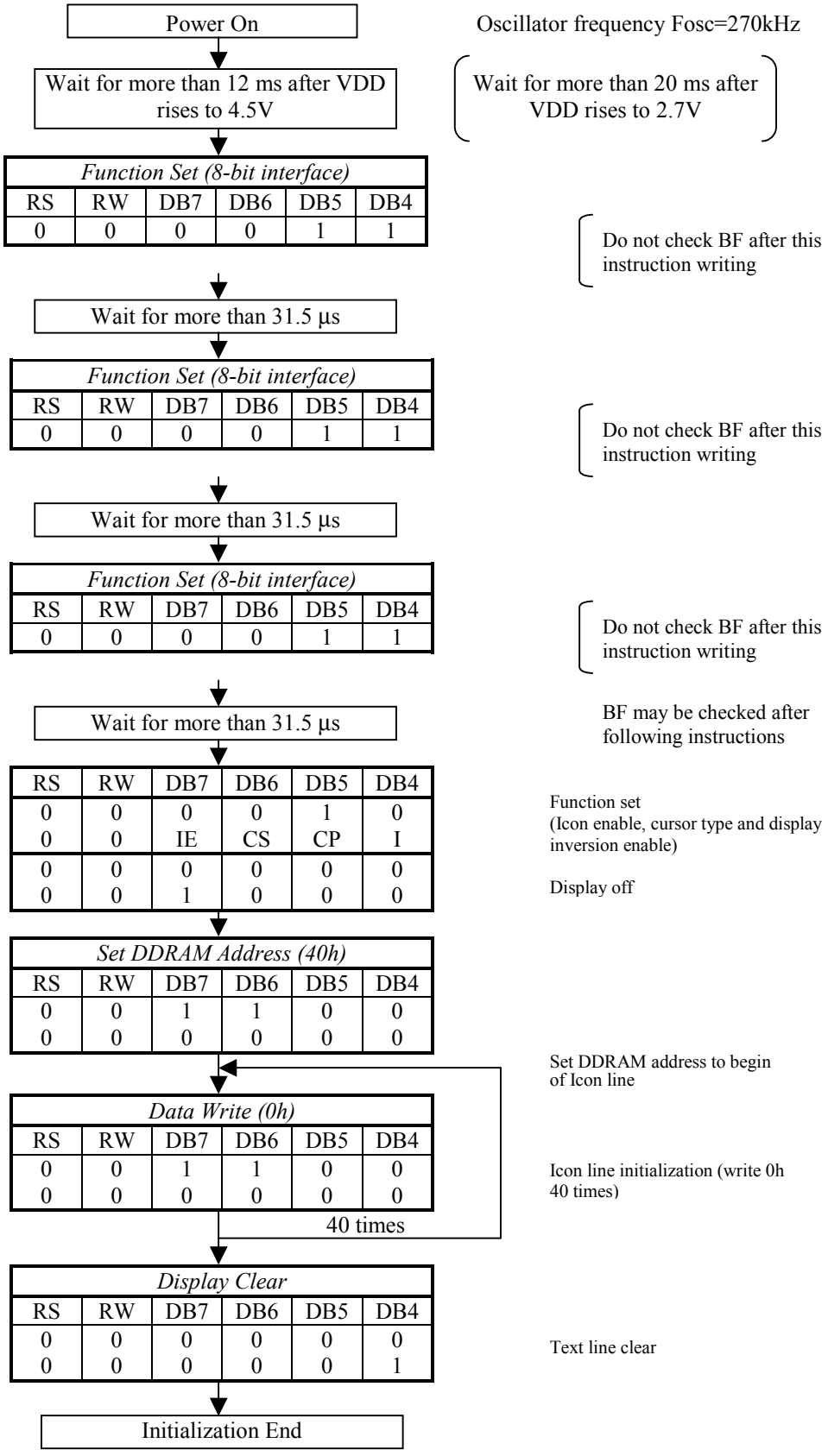


Figure 32. Initializing by instruction in the Large Font and 4-bit interface mode

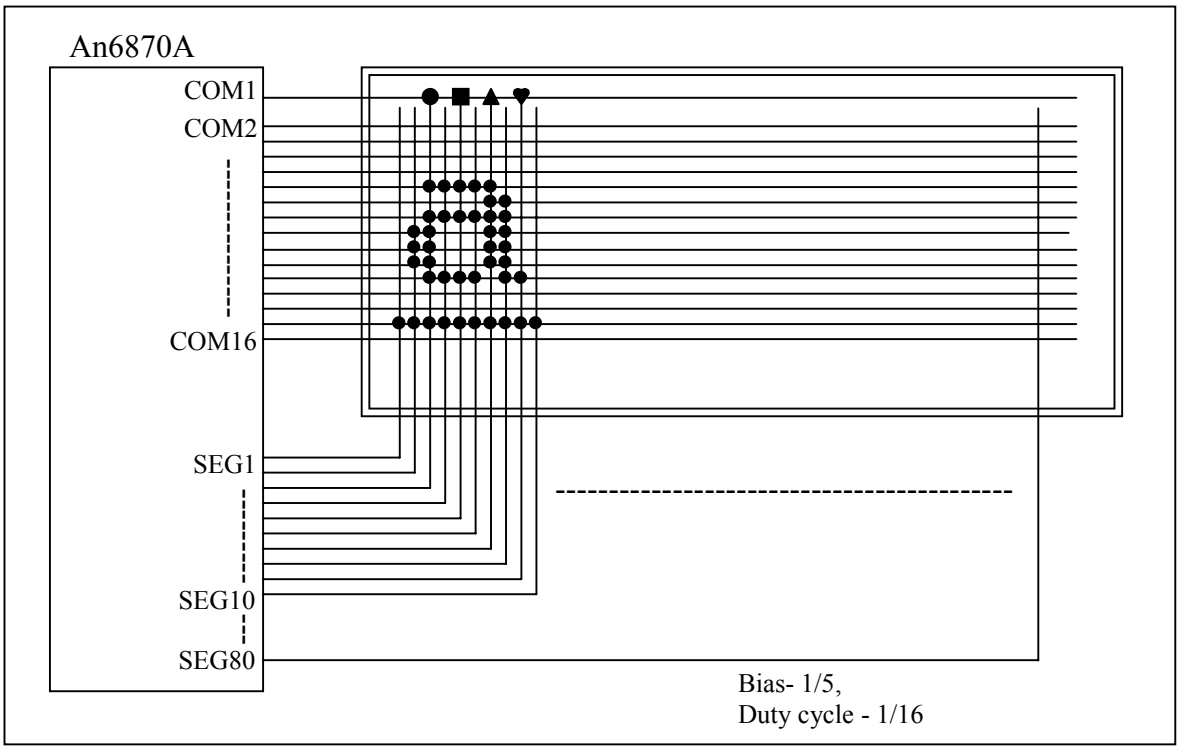


Figure 33. Example of 10x15 dots, 8 character x 1 line display.

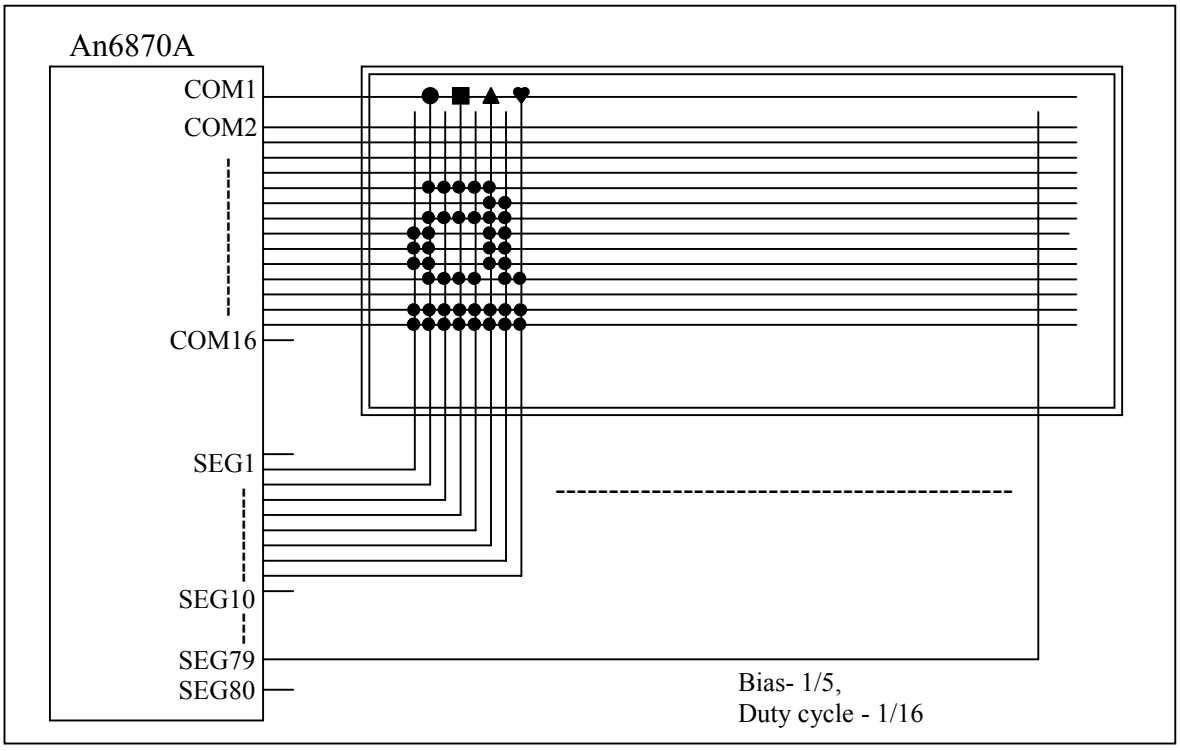


Figure 34. Example of 8x14 dots, 8 character x 1 line display with double-size cursor.

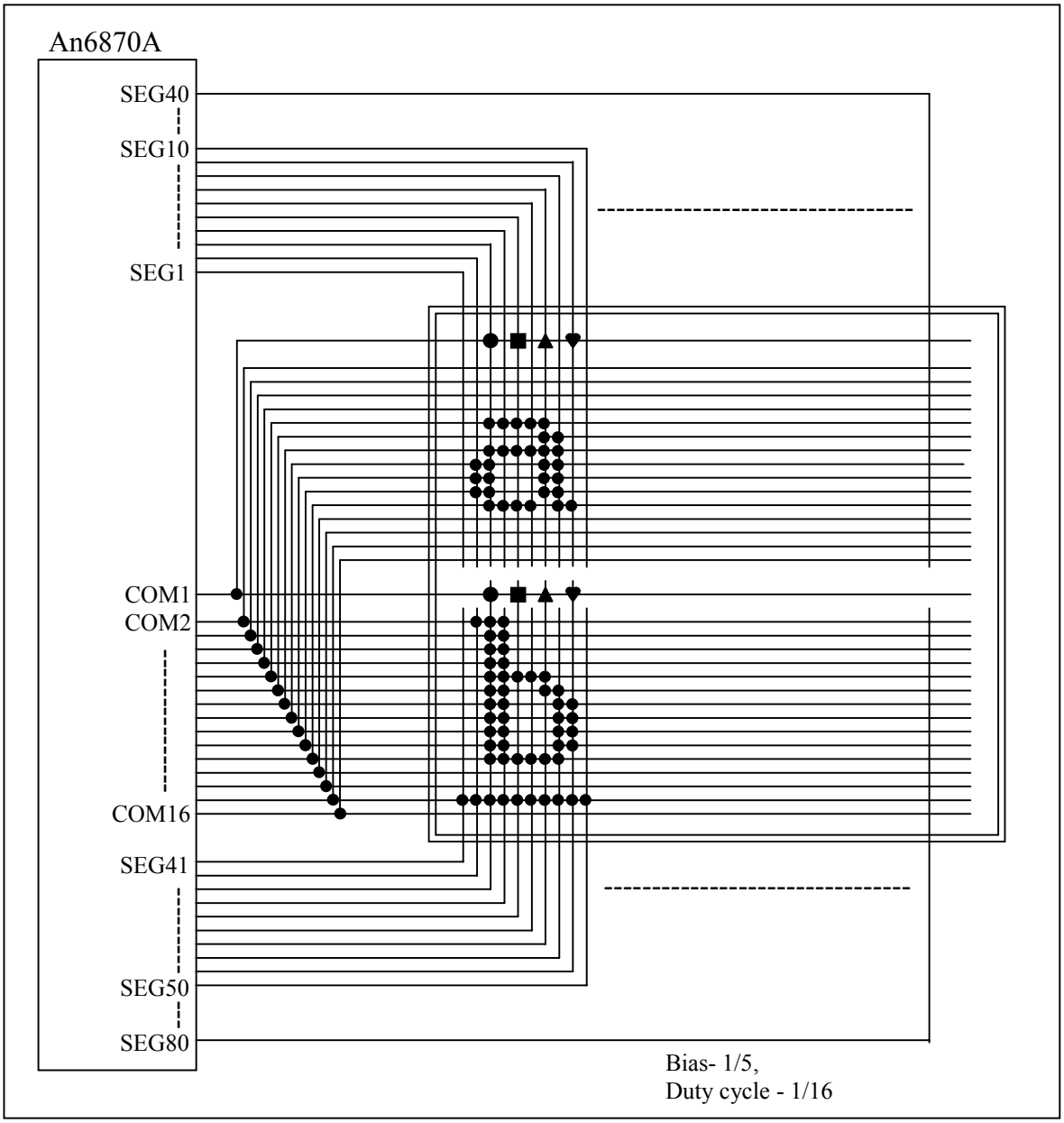


Figure 35. Example of 10x15 dots, 4 character x 2 line display.

APPENDIX 1

An6870 Order Form for Standard and Extended Modes

Function	Standard Mode XMODE=1	Extended Mode XMODE=0	Comments
1. Standard CGROM mask option	☐		This parameter is specified only when one of the standard CGROM mask options is selected. When the customer's own code is ordered, a respective form is to be attached hereto and this parameter is omitted (dash instead).
2. Two CGROM pages selection	☐ – yes ☐ – no	☐ – yes ☐ – no	Selection of two CGROM pages is enabled either in extended mode or in two modes simultaneously.
	☐ – fixed pages		
3. Starting address of 2nd CGROM page. 4. Final address of 2nd CGROM page	☐ ☐		The starting and final addresses of 2nd CGROM page are set when selection of two CGROM pages (i.2) is enabled at least in one of the modes. The addresses of table columns are specified either in hex, or decimal or binary form (suffixes h, d, or b respectively). Example: 0E h, 14 d, 1110 b
5. Display Inverse enable	☐ – yes ☐ – no	☐ – yes ☐ – no	Enabling of program control for display inversion or setting of fixed inversion mode. Enabled either in extended mode or in two modes simultaneously.
	☐ - fixed Inverse mode		
6. CGROM characters for 08h-0Fh codes	☐ – yes ☐ – no		Selection of CGROM characters to 08h-0Fh addresses. Allows increase of CGROM characters up to 248. Can be set only for two modes simultaneously.
7. Cursor blink enable	☐ – yes ☐ – no	☐ – yes ☐ – no	Setting of blinking cursor with Cursor On and Blink On simultaneously. Enabled either in extended mode or in two modes simultaneously.
8. COM & SEG waveform type	☐ – A-type ☐ – B-type	☐ – A-type ☐ – B-type	Setting of display control at COM & SEG outputs: change of voltage polarity in each COM cycle (type A) or in the whole display refresh cycle (type B).
9. Basic modes selection: - Interface data length - Number of display lines - Font size	☐ – 4 bits (Power On Reset) ☐ – 8 bits (Power On Reset) ☐ – 4 bits (Fixed) ☐ – 8 bits (Fixed) ☐ – 1 COM line (Power On Reset) ☐ – 2 COM lines (Power On Reset) ☐ – 1 COM line (Fixed) ☐ – 2 COM lines (Fixed) ☐ – 5x8 (Power On Reset) ☐ – 5x11 (Power On Reset) ☐ – 5x8 (Fixed) ☐ – 5x11 (Fixed)		Selection of initial state of basic mode parameters or their fixing in a definite state (without program control). The parameter can be fixed when the alternative state for this configuration is not required. For example, if 5x11 dot format is coded in CGROM, only this font size and number of COM lines can be fixed as no other size is available. These parameters can be set for both modes simultaneously.

Customer _____ / /

"___" _____ 200_ .

APPENDIX 2

An6870A Order Form for Large Font Mode

Function	XMODE=1	XMODE=0	Comments
1. Standard CGROM mask option	☐		This parameter is specified only when a standard CGROM mask option is selected. If the customer orders his own code, a respective form is attached hereto and this parameter is omitted (dash instead).
2. Display Inverse enable	☐ – yes ☐ – no	☐ – yes ☐ – no	Setting program controlled or fixed Inverse mode. Enabled either in extended mode or in two modes simultaneously.
	☐ - Fixed Inverse mode		
3. COM and SEG waveform type	☐ – A-type ☐ – B-type	☐ – A-type ☐ – B-type	Providing screen control at COM and SEG outputs: voltage polarity is changed in every COM cycle (A-type) or in the whole screen refresh cycle (B-type).
4. Basic mode selection - Interface data length	☐ – 4 bits (Power On Reset) ☐ – 8 bits (Power On Reset) ☐ – 4 bits (fixed) ☐ – 8 bits (fixed)		Selection of the initial state of basic mode parameters or their fixation in a certain state (without program control function). A fixed interface data length is used if the alternative state is not required for a given configuration. This parameter can be set simultaneously for both modes.
- Cursor size	☐ – 1 COM line (Power On Reset) ☐ – 2 COM lines (Power On Reset)		The cursor can occupy one or two COM lines. This parameter can be set simultaneously for both modes.
- Cursor position	☐ – 16-th COM line (Power On Reset) ☐ – 15-th COM line (Power On Reset)		The cursor starting position can be the 16-th or 15-th COM line. In case of the two-line cursor it can be located in lines 16&15 or 15&14, respectively. This parameter can be set for both modes simultaneously.

Customer _____ / /

"___" _____ **200_ .**

APPENDIX 3

CGROM Pattern Form for Standard and Extended Modes (for An6870)

1st CGROM page (font 5x8 and 5x11)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	(0)															
1	(1)															
2	(2)															
3	(3)															
4	(4)															
5	(5)															
6	(6)															
7	(7)															
8																
9																
A																
B																
C																
D																
E																
F																

Customer _____ / ..... /

"___" _____ **200_ .**

CGROM Pattern Form for Standard and Extended Modes (for An6870)

2nd CGROM page (font 5x8)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	(0)															
1	(1)															
2	(2)															
3	(3)															
4	(4)															
5	(5)															
6	(6)															
7	(7)															
8																
9																
A																
B																
C																
D																
E																
F																

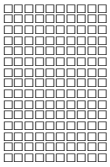
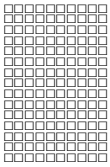
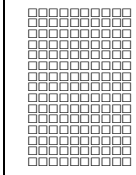
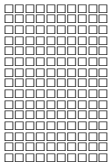
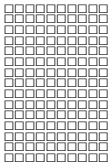
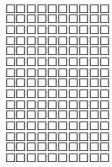
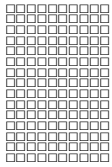
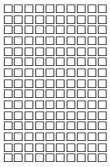
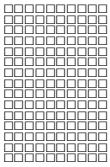
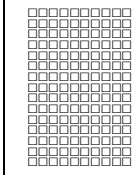
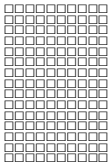
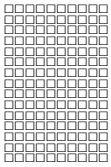
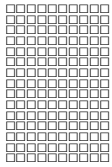
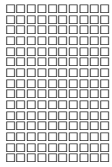
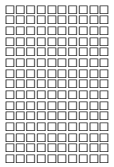
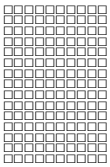
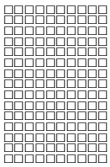
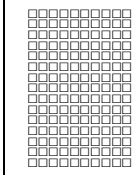
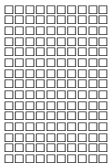
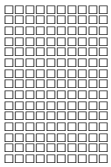
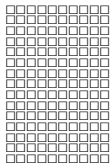
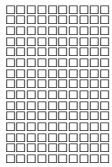
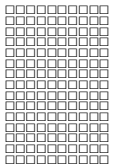
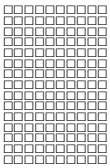
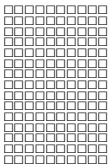
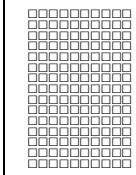
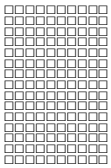
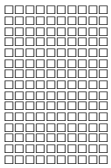
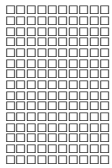
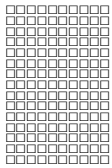
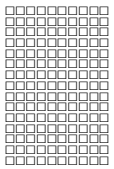
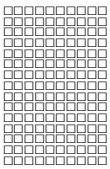
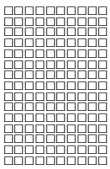
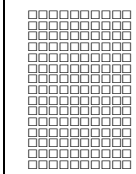
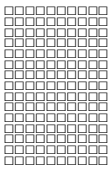
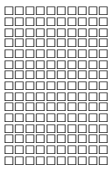
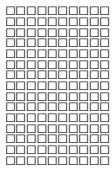
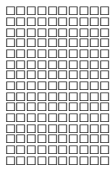
Customer _____ / ..... /

"___" _____ 200_

APPENDIX 4

CGROM Pattern Form for Large Font Mode (for An6870A)

1/2 page (font 10x15)

	0	1	2	3	4	5	6	7
0								
1								
2								
3								
4								
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CGROM Pattern Form for Large Font Mode (for An6870A)

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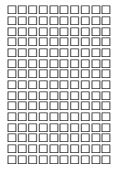
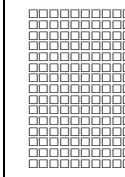
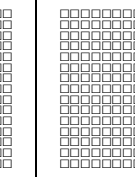
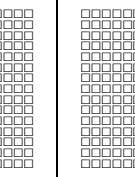
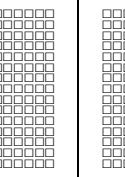
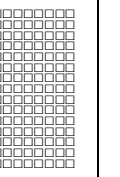
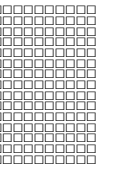
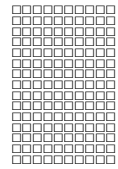
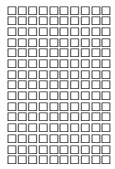
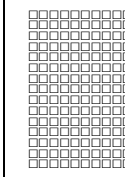
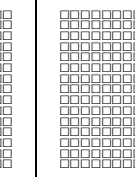
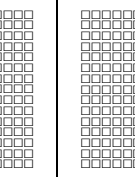
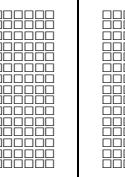
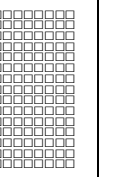
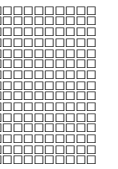
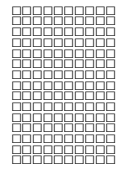
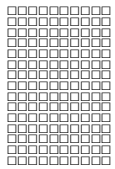
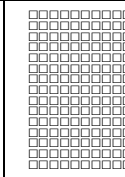
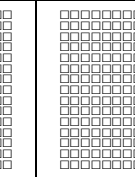
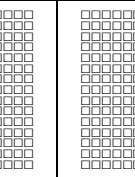
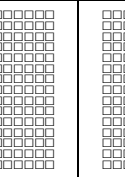
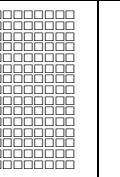
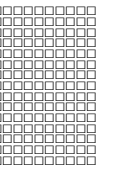
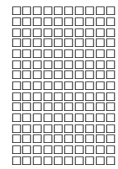
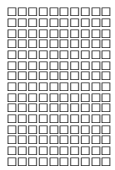
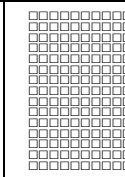
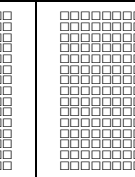
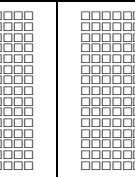
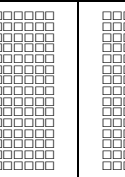
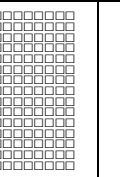
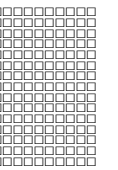
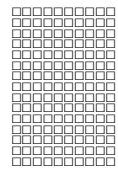
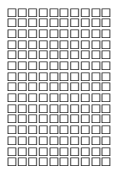
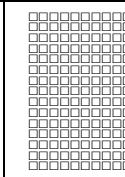
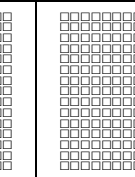
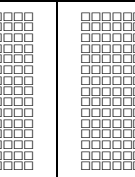
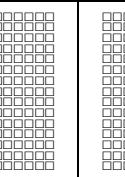
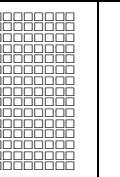
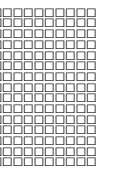
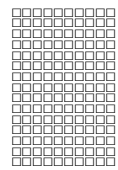
8								
9								
A								
B								
C								
D								
E								
F								

Customer _____ / ..... /

"___"_____200_

APPENDIX 5

Released CGROM Patterns

S00 pattern. 2nd page start address..... 1h
2nd page end address..... Dh
using 08h-0Fh code range for CGROM..... no

Page 1

Lower 4-bit (D0 to D3) of Character Code (hex.)	Higher 4-bit (D4 to D7) of Character Code (hex.)															
	Ø	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Ø	CG RAM (1)															
1	CG RAM (2)															
2	CG RAM (3)															
3	CG RAM (4)															
4	CG RAM (5)															
5	CG RAM (6)															
6	CG RAM (7)															
7	CG RAM (8)															
8	CG RAM (1)															
9	CG RAM (2)															
A	CG RAM (3)															
B	CG RAM (4)															
C	CG RAM (5)															
D	CG RAM (6)															
E	CG RAM (7)															
F	CG RAM (8)															

S00 pattern

Page 2 **Characters in E, F columns are selected from 1st page**

L00 pattern (Large Font)

Lower 4-bit (D0 to D3) of Character Code (hex.)	Higher 4-bit (D4 to D7) of Character Code (hex.)							
	Ø	1	2	3	4	5	6	7
Ø	CG RAM (1)	¢		0	@	P	`	p
1	CG RAM (2)	£	!	1	A	Q	a	q
2	α	2	"	2	B	R	b	r
3	β	3	#	3	C	S	c	s
4		¼	$	4	D	T	d	t
5	€	⅓	%	5	E	U	e	u
6	μ	½	&	6	F	V	f	v
7		⅔	'	7	G	W	g	w
8	ρ	¾	(	8	H	X	h	x
9	π	№	)	9	I	Y	i	y
A		÷	*	:	J	Z	j	z
B		±	+	;	K	[	k	{
C	Σ	ä	,	<	L	¥	l	|
D		ö	-	=	M	]	m	}
E		ü	.	>	N	^	n	→
F		ß	/	?	O	_	o	←

APPENDIX 6

Released Mask Options of An6870

An6870-0000

Parameter	Standard Mode XMODE=1	Extended Mode XMODE=0
1. CGROM pattern	S00	
2. CGROM page	1st page	Software controlled (P bit of Function Set instruction)
5. Display inversion enabling	no	Software controlled (I bit of Function Set instruction)
7. Underline cursor blinking enable	no	yes
8. Display Waveform type	A-type	B-type
9. Function Set:		
- Interface data bus width	8 bit (init)	
- Number of display lines	1 line (init)	
- Font size	5x8 (init)	

Address		Identification Code of An6870-0000									Parameter
Dec.	Hex.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Value (hex)	
120	78	0	1	0	0	0	0	0	1	65	Chip Identifier
121	79	0	1	0	0	1	1	1	0	78	
122	7A	0	1	0	0	0	1	0	0	68	
123	7B	0	1	0	0	0	1	1	0	70	
124	7C	0	0	0	0	0	0	0	0	00	CGROM version
125	7D	0	0	0	0	0	1	0	1	05	Configuration
126	7E	0	0	0	1	0	1	P	I	*	Config./Current state
127	7F	X	N	F	D	C	B	ID	SH	*	Current state

An6870A-5000

Parameter	XMODE=1	XMODE=0
1. Large Font mode	yes	
2. CGROM pattern	L00	
3. Display inversion enabling	no	software controlled
4. Underline cursor blinking enable	yes	yes
5. Display Waveform type	B-type	B-type
6. Function Set:		
- Interface data bus width	8 bit (init)	
- Icon displaying	No (init)	
- Cursor position	COM15	
- Cursor size	1 COM-line	

Address		Identification Code of An6870A-5000									Parameter
Dec.	Hex.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Value (hex)	
120	78	0	1	0	0	0	0	0	1	65	Chip Identifier
121	79	0	1	0	0	1	1	1	0	78	
122	7A	0	1	0	0	0	1	0	0	68	
123	7B	0	1	0	0	0	1	1	0	70	
124	7C	0	0	0	0	0	0	0	0	00	CGROM version
125	7D	0	0	0	0	0	0	0	1	01	Configuration
126	7E	1	0	1	1	1	1	P	I	*	Config./Current state
127	7F	X	N	F	D	C	B	ID	SH	*	Current state