Winbond Electronics Corp.

4-BIT MICROCONTROLLER

Table of Contents-

1. GENERAL DESCRIPTION

The W921E840 is a single-chip CMOS 4-bit microcontroller that is a subset of W921E880. It features four multi-function timers, one channel DTMF generator, an 8-bit D/A converter circuit, eight interrupt sources, 48-level subroutine nesting, and built in four by one channel comparator circuit. Two power down modes, hold and stop mode, reduce power dissipation. The excellent memory structure, 8K super EPROM for program code and 512 x 4 bit RAM minimize the need for external memory devices.

W921E840 is a powerful microcontroller for wide range consuming applications, requiring few external components, which is especially suited for telecommunication design.

2. FEATURES

Operating Voltage

- 2.7 to 5.5 V operating voltage

Operating Frequency

- Crystal or RC for main system clock
  - Crystal for 400K, 800K, 2M, 3.58M, 4MHz
  - RC up to 4MHz

Memory

- 8K × 10-bit ROM (super EPROM)
- 512 × 4-bit RAM
  - 64 × 4-bit special registers
  - 16 × 4-bit working registers
  - 128 × 4-bit general registers
  - 304 × 4-bit multi-purpose registers

Stack

- 8-bit stack pointer

I/O Pins

- 20 bidirectional and individually controllable I/O lines
  - P2 Port: P2.0 to P2.3 large sink current pins and open drain option
  - P3 Port: P3.0 to P3.3 multi-function I/O
  - P4 Port: P4.0 to P4.3 open drain and pull high resistor option, multi-function I/O
  - P5 Port: P5.0 to P5.3 multi-function I/O
  - P6 Port: P6.0 to P6.3 open drain and pull high resistor option, multi-function I/O
- 14 bidirectional I/O lines
  - PA Port: PA.0 to PA.3 open drain and pull high resistor option

– PB Port: PB.0 to PB.3 open drain and pull high resistor option

– PC Port: PC.1 to PC.3 open drain and pull high resistor option

– PD Port: PD.0 to PD.1 open drain and pull high resistor option

Serial I/O Interface

- Clock synchronous multi-nibbles serial transmitter/receiver interface

DTMF Generator

- One channel DTMF generator

Beep Tone Generator

- One channel beep tone generator

8-bit D/A Converter

- One channel 8-bit D/A converter

Voltage Comparator

- Multiplexed four channel voltage comparator

Timer/Counter

- Timer 0: 2 to 19 order divider, auto-reload timer, watch-dog timer
- Timer 1: 2 to 19 order divider, auto-reload timer, arbitrary waveform generator, external event counter
- Timer 2: 2 to 19 order divider, auto-reload timer, arbitrary waveform generator, period/pulse width measurement function
- Timer 3: 2 to 19 order divider, auto-reload timer

Interrupt

- Two external sources: INT0 (P4.3), P4 Port (P4.0 to P4.2)
- Six internal sources: Timer 0, Timer 1, Timer 2, Timer 3, Comparator, Serial Port

Operating Mode (System Clock)

- Normal mode: system clock operating
- HOLD mode: no operation except for oscillator (system clock stops only)
- STOP mode: no operation including oscillator

Addressing Mode

- ROM: Short jump addressing mode

Indirect Call Addressing Mode

Long jump/call addressing mode

- RAM: Direct addressing mode

Indirect Addressing Mode

Working register addressing mode

- Look-up table addressing mode

Instruction Sets

- 108 instruction sets

Package Type

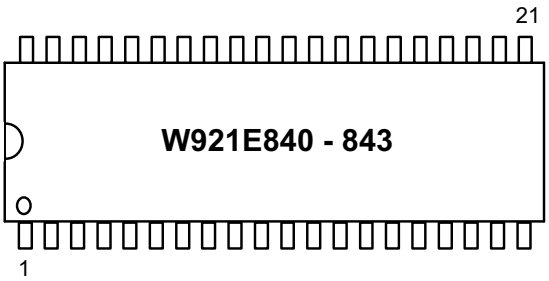
- 40-pin DIP, 48-pin QFP

The W921E840 microcontroller series are shown in the following table:

PART NO.	PACKAGE TYPE	FUNCTION
W921E840	40-pin DIP	With pin PD.0, PD.1, BTG without dual clock $\overline{XT}$, XT, PC.0
W921E841	40-pin DIP	With dual clock $\overline{XT}$, XT, PC.0 without pin PD.0, PD.1, BTG
W921E842	40-pin DIP	With pin PD.0, PD.1, PC.0 without dual clock $\overline{XT}$, XT, BTG
W921E843	40-pin DIP	With dual clock $\overline{XT}$, XT, BTG without pin PD.0, PD.1, PC.0
W921E844	48-pin QFP	With pin PD.0, PD.1, PC.0, BTG, dual clock $\overline{XT}$, XT

3. PIN CONFIGURATION

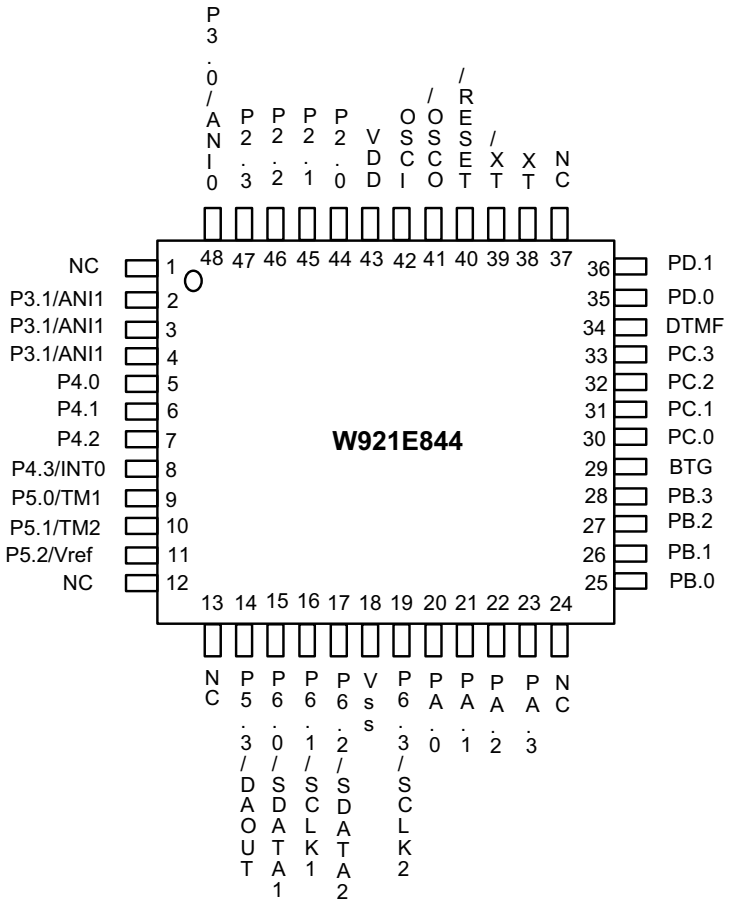
40-pin DIP



PIN NAME	DIP40	PIN NAME	DIP40
P2.0	1	P6.3/SCLK2	21
P2.1	2	PA.0	22
P2.2	3	PA.1	23
P2.3	4	PA.2	24
P3.0/ANI0	5	PA.3	25
P3.1/ANI1	6	PB.0	26
P3.2/ANI2	7	PB.1	27
P3.3/ANI3	8	PB.2	28
P4.0	9	PB.3	29
P4.1	10	PC.0 or BTG	30
P4.2	11	PC.1	31
P4.3/INT0	12	PC.2	32
P5.0/TM1	13	PC.3	33
P5.1/TM2	14	DTMF	34
P5.2/VREF	15	PD.0 or XT	35
P5.3/DAOUT	16	PD.1 or $\overline{XT}$	36
P6.0/SDATA1	17	$\overline{RESET}$	37
P6.1/SCLK1	18	$\overline{OSCO}$	38
P6.2/SDATA2	19	OSCI	39
VSS	20	VDD	40

3. Pin Configuration, continued

48-pin QFP



PIN NAME	QFP 48	PIN NAME	QFP 48
NC	1	PB.0	25
P3.1/ANI1	2	PB.1	26
P3.2/ANI2	3	PB.2	27
P3.3/ANI3	4	PB.3	28

Continued

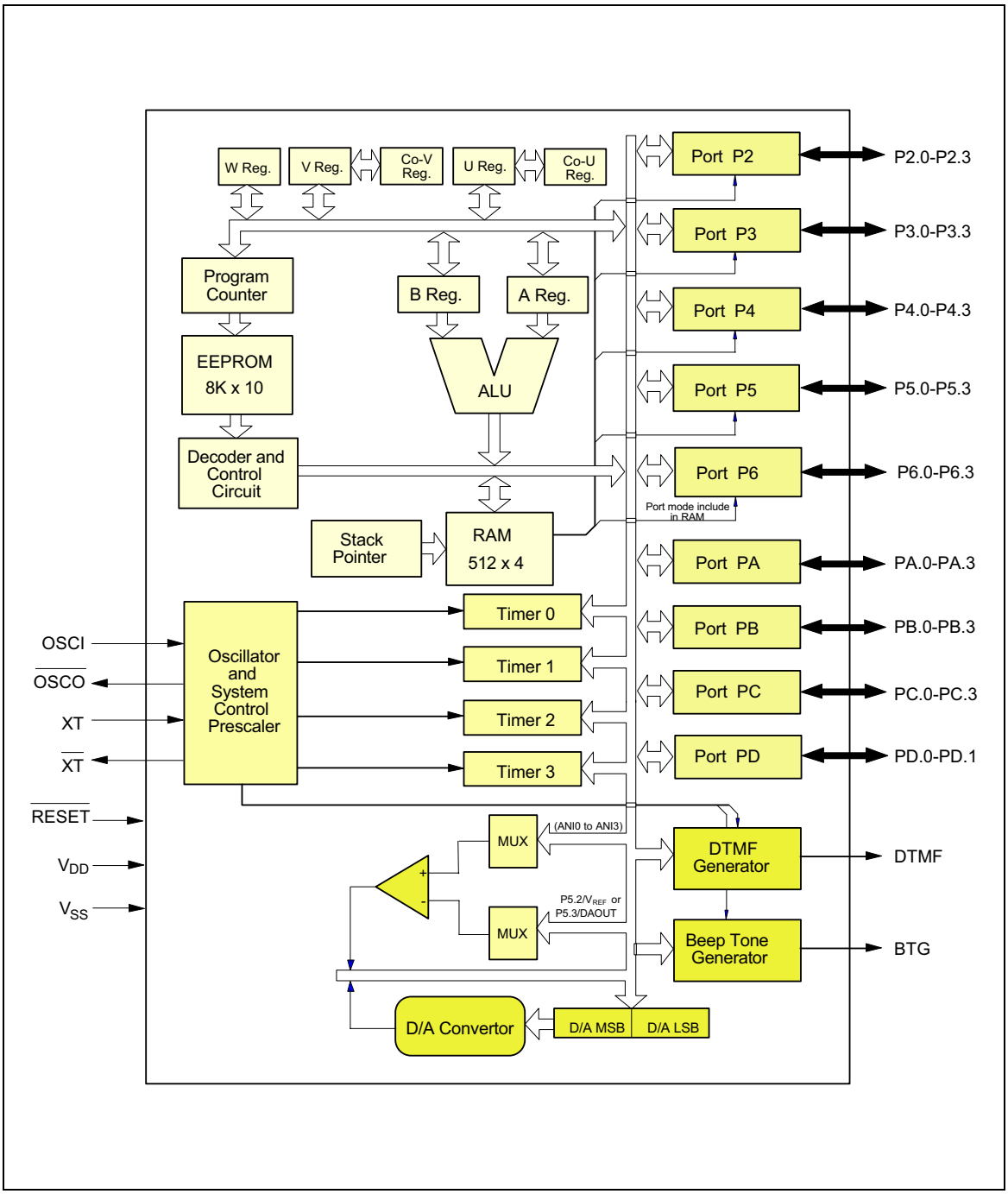
PIN NAME	QFP 48	PIN NAME	QFP 48
P4.0	5	BTG	29
P4.1	6	PC.0	30
P4.2	7	PC.1	31
P4.3/INT0	8	PC.2	32
P5.0/TM1	9	PC.3	33
P5.1/TM2	10	DTMF	34
P5.2/VREF	11	PD.0	35
NC	12	PD.1	36
NC	13	NC	37
P5.3/DAOUT	14	XT	38
P6.0/SDATA1	15	$\overline{XT}$	39
P6.1/SCLK1	16	$\overline{RESET}$	40
P6.2/SDATA2	17	$\overline{OSCO}$	41
VSS	18	OSCI	42
P6.3/SCLK2	19	VDD	43
PA.0	20	P2.0	44
PA.1	21	P2.1	45
PA.2	22	P2.2	46
PA.3	23	P2.3	47
NC	24	P3.0/ANI0	48

4. PIN DESCRIPTION

SYMBOL	I/O	FUNCTION	EPROM FUN.✣
OSCI	I	Main oscillator input pin with internal capacitor	VPP
$\overline{\text{OSCO}}$	O	Main oscillator output pin	$\overline{\text{PROG}}$
P2.0 to P2.3	I/O✶	I/O port 2 with large sink current	
P3.0/ANI0 to P3.3/ANI3	I/O	I/O port 3 or analog input (ANI0 to ANI3) pins	A10, A11, A12, $\overline{\text{PROGD}}$ / $\overline{\text{ERASE}}$
P4.0	I/O✶	I/O pin P4.0 or the input pin of interrupt port	
P4.1	I/O✶	I/O pin P4.1 or the input pin of interrupt port	
P4.2	I/O✶	I/O pin P4.2 or the input pin of interrupt port	
P4.3/INT0	I/O✶	I/O pin P4.3 or INT0 input pin	
P5.0/TM1	I/O	I/O pin P5.0 or the controlled pin of timer 1	
P5.1/TM2	I/O	I/O pin P5.1 or the controlled pin of timer 2	
P5.2/VREF	I/O	I/O pin P5.2 or the VREF input pin of the comparator	
P5.3/DAOUT	I/O	I/O pin P5.3 or the output pin of 8-bit D/A converter	
P6.0/SDATA1	I/O✶	I/O pin P6.0 or the data I/O pin of serial interface	A8/D8
P6.1/SCLK1	I/O✶	I/O pin P6.1 or the clock I/O pin of serial interface	A9/D9
P6.2/SDATA2	I/O☆	I/O pin P6.2 or the data I/O pin of serial interface	$\overline{\text{READ}}$
P6.3/SCLK2	I/O✶	I/O pin P6.3 or the clock I/O pin of serial interface	LATCH
PA.0 to PA.3	I/O✶	I/O port A with wake up stop mode function	A0/D0 to A3/D3
PB.0 to PB.3	I/O✶	I/O port B with wake up stop mode function	A4/D4 to A7/D7
PC.0 to PC.3	I/O✶	I/O port C	
PD.0 or $\overline{\text{XT}}$	I/O✶	I/O pin PD.0 or 32.768 KHz subsystem clock input pin (with internal capacitor)	
PD.1 or XT	I/O✶	I/O pin PD.1 or 32.768 KHz subsystem clock input pin	
DTMF	O	Dual tone multi-frequency output pin	
BTG	O	Beep tone generator output pin	
$\overline{\text{RESET}}$	I	Reset input pin with low active	$\overline{\text{RESET}}$
VDD	I	Positive power supply input pin	VDD
VSS	I	Negative power supply input pin	VSS

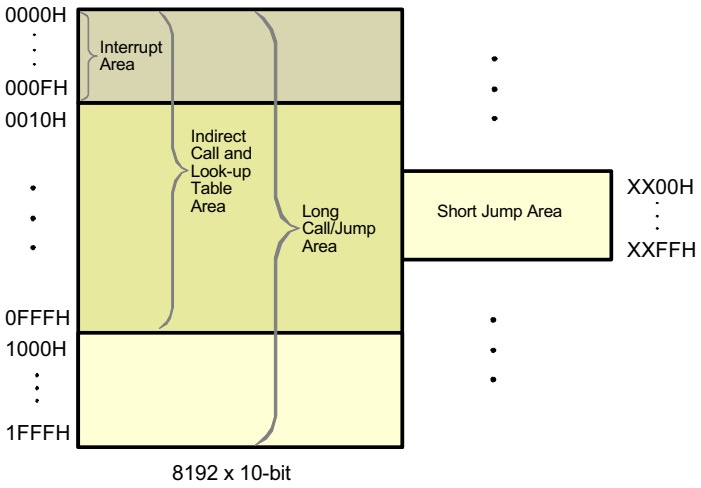
Notes:
- ✣ for more details, refer to EPROM function
- ✶ open drain option by software
- ☆ open drain and pull high resistor option by software

5. BLOCK DIAGRAM



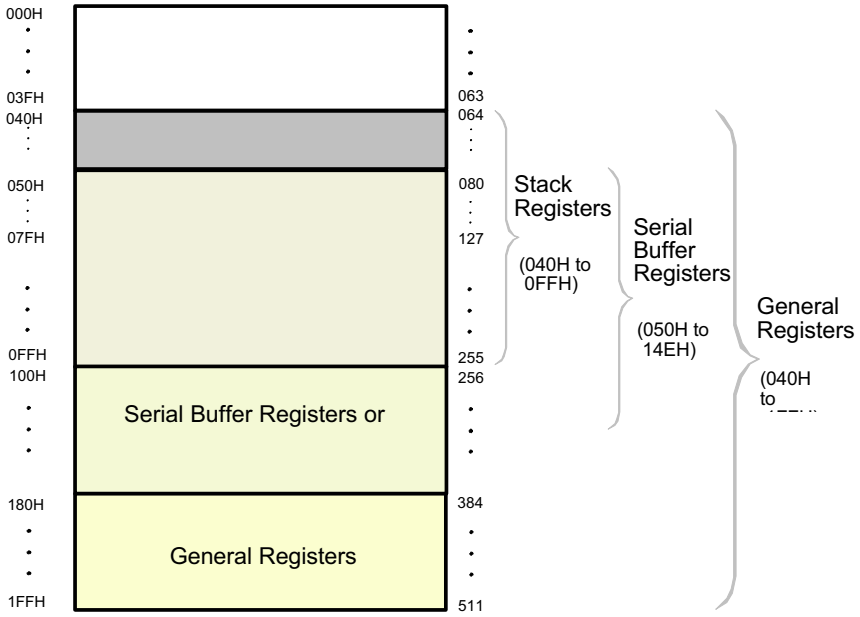
6. FUNCTIONAL DESCRIPTION

6.1 ROM Memory Map



0000H	JMPL Instruction (Reset)
	XXXXX XXXXX
0002H	
0003H	XXXXX XXXXX
	JMPL Instruction (TM0)
0005H	
0006H	JMPL Instruction (TM1)
	XXXXX XXXXX
0008H	
0009H	XXXXX XXXXX
	JMPL Instruction (Comparator / TM3)
000BH	
000CH	JMPL Instruction (P4.0 to P4.2)
	XXXXX XXXXX
000EH	
000FH	XXXXX XXXXX

6.2 RAM Memory Map



(512 x 4-bit)

6.2.1 Special Control Register Area

There are 64 × 4-bit registers in the special control register area. All control registers such as DTMF control register, serial speed control register, ..., etc. are in this area. Please refer to the following table for detailed register map.

ADDR.	DESCRIPTION	ABBREVIATION	INITIAL VALUE
000H	Reserved or System Clock Control Register	(SYSCCR)	00H
001H	Bank Select Register	(BKSR)	02H
002H	Reserved	-	-
003H	Port P4 Pull High Resistor Register	(P4PH)	00H
004H	Port P4 Output Type Register	(P4TP)	00H
005H	Port P6 Pull High Resistor Register	(P6PH)	00H
006H	Port P6 Output Type Register	(P6TP)	00H
007H	Port PABCD Pull High Resistor Register	(PABCDPH)	00H
008H	Port PABCD Output Type Register	(PABCDTP)	00H
009H	Serial LSB Nibble Register	(SRLNR)	02H

6.2.1 Special Control Register Map, continued

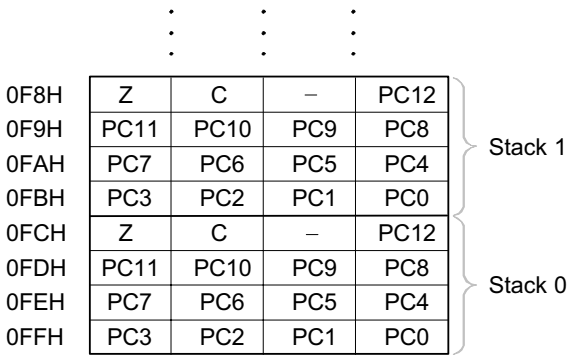
	DESCRIPTION	ABBREVIATION	
00AH	Serial MSB Nibble Register		00H
00BH		(SRSPC)	00H
	Serial Clock Inverter Control Register	(SRINV)	
00DH	Port P2 Output Type Register		00H
00EH			-
00FH		(P3IO)	00H
	Port P4 I/O Status Control Register	(P4IO)	
011H	Port P5 I/O Status Control Register		00H
012H		(P6IO)	00H
	DTMF Oscillation Control Register	(OSCCTR)	
014H	DTMF Register		00H
015H		(RCCTL)	00H
	D/A Control Register	(DACTL)	
017H	D/A Converter LSB Data Register		00H
018H		(DAMSB)	00H
	Comparator Analog Input Multiplexer	(ANIMUX)	
01AH	Comparator Control Register		04H
01BH			-
01CH		(TM1RM)	0FH
	TM1 Read Only LSB Data Register	(TM1RL)	
01EH	TM2 Read Only MSB Data Register		0FH
01FH		(TM2LM)	0FH
	TM0 Control Register	(TM0CR)	
021H	TM0 MSB Data Register		0FH
022H		(TM0LSB)	0FH
	TM0 Status Register	(STTM0)	
024H	Reserved or Timer 0 Low Speed Register		00H
025H		(TM1CR)	00H
	TM1 MSB Data Register	(TM1MSB)	
027H	TM1 LSB Data Register		0FH
028H		(STTM1)	00H
	TM1 Trigger Condition Register	(TGTM1)	
02AH	TM2 Control Register		00H
02BH		(TM2MSB)	0FH

6.2.1 Special Control Register Map, continued

	DESCRIPTION	ABBREVIATION	
02CH	TM2 LSB Data Register		0FH
02DH		(STTM2)	00H
	TM2 Trigger Condition Register	(TGTM2)	
02FH	TM3 Control Register		00H
030H		(TM3MSB)	0FH
	TM3 LSB Data Register	(TM3LSB)	
032H	TM3 Status Register		00H
033H			-
034H		(ENINT)	00H
	Stop Mode Released Flag	(STPRF)	
036H	Hold Mode Released Flag 1		00H
037H		(HMRF2)	00H
	Hold Mode Released Flag 3	(HMRF3)	
039H	Interrupt Control Register 1		00H
03AH		(INTCT2)	00H
	Interrupt Control Register 3	(INTCT3)	
03CH	Hold Released Status Flag 1		00H
03DH		(HRSTS2)	00H
	Hold Released Status Flag 3	(HRSTS3)	
03FH	Beep Tone Generator Register		00H

6.2.2 Stack Register Area

stack pointer will be set to 0FFH. The stack pointer will be decreased by 4 when the CALL/ CALLP or interrupt is accepted, and will be increased by 4 when the RTN or RTNI instruction is executed. The



6.2.3 Working Register Area

The located area from 040H to 04FH is known as working register. The instruction MOV WRn, A or MOV A, WRn can move the A accumulator data to the working register or move working register data to the A accumulator directly within the 1 word / 1 machine cycle. The other direct instructions such as MOV Mx, A or MOV A, Mx instruction are 2 words / 2 machine cycles. Therefore the working register can save the program memory size in ROM and improve the control speed in μC application circuit.

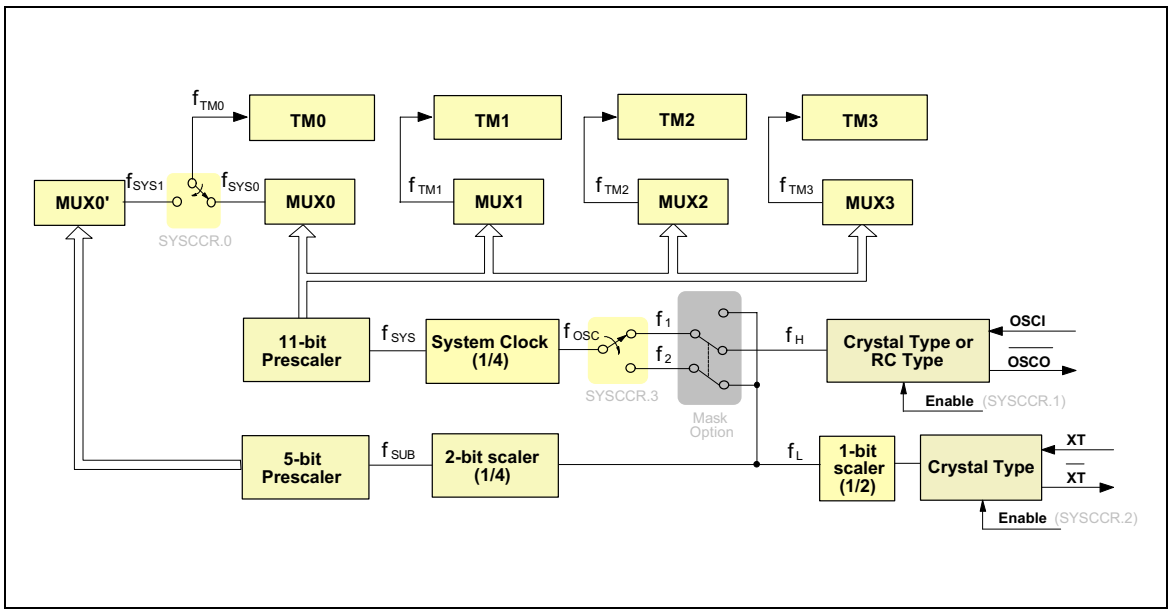
Only the WR0 to WR7 are available in the arithmetic and logic operation (I. e. only 040H to 047H can be active). The instructions are as follows:

```
ADD   A,   WRx
ADC   A,   WRx
SUB   A,   WRx
SBC   A,   WRx
ANL   A,   WRx
ORL   A,   WRx
XRL   A,   WRx
CMP   A,   WRx
```

where x = 0 to 7.

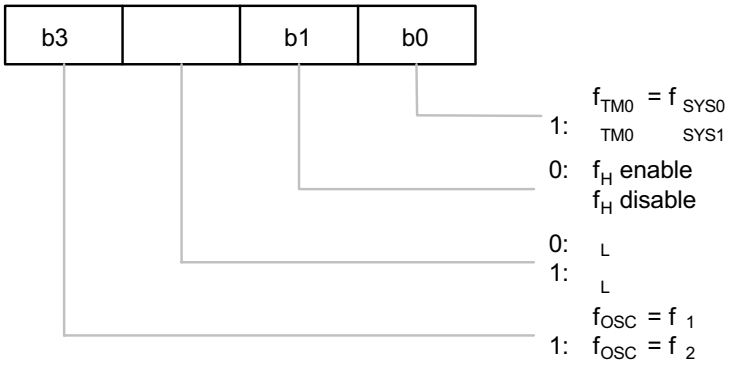
6.3 Internal Oscillator Circuit

There are dual clocks in this chip, one high speed, the other low speed. The block diagram is shown below:

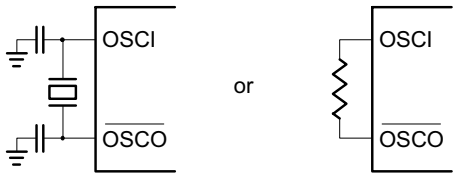


The detail function of the system clock control register (SYSCCR) is shown as below:

SYSCCR register: (address = 000H, default data = 0H, only for W921E841, 843, 844)



The W921E840 provides a crystal or RC oscillation circuit selected by bit0 of INI1 register (refer to section 7.1) to generate the system clock through external connections. If a crystal oscillator is used, a crystal or ceramic resonator must be connected to OSCI and $\overline{OSCO}$, and the capacitor is added optionally. The oscillator configuration is shown as follows.



6.4 Initial State

The W921E840 is reset either by a power-on reset or by using the external $\overline{RESET}$ pin. The initial state of the W921E840 after the reset function is executed is described below.

Program counter (PC)	0000H
Stack pointer	0FFH
Special function registers	Refer to section 6.2.1
TM0, TM1, TM2, TM3 input clock	Fosc/8
TM0, TM1, TM2, TM3 contents	0FFH
Input/Output	Input mode
PM registers	1111B
DTMF output	Disable (H-Z)

6.5 Input/Output

There are 34 I/O pins including 4 large sink current pins in this chip. All the I/O pins will remain in the input mode after power on reset.

The I/O instructions are described as follows:

MOV	A, Px	Input port x to A accumulator
MOV	B, Px	Input port x to B accumulator
MOV	Px, A	Output A accumulator data to port x.
MOV	Px, B	Output B accumulator data to port x.

The input or output status of port 2 to port 6 can be pin controlled by port mode register (PMx, where x = 2 to 6). Data 0 of PMx indicates the corresponding pin as output mode, and data 1 indicates the relative pin as input mode. For example, MOV PM2, #0101B, it sets P2.0 and P2.2 in input mode and P2.1 and P2.3 in output mode. The I/O instructions don't affect the I/O status in Port 2 to Port 6.

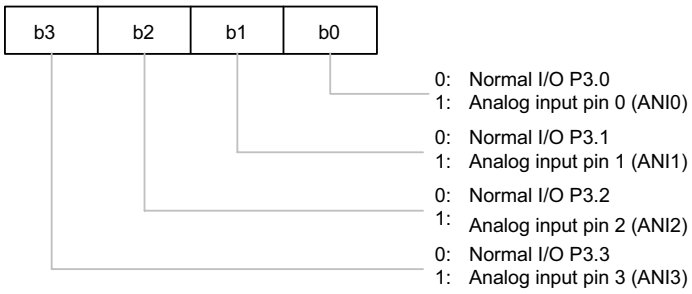
The input or output mode of port A to port D only can be decided by I/O instructions. For example, MOV A, Px will change Px to input mode and MOV Px, A will change it to output mode.

6.5.1 Normal/Special Function Selection of I/O

Some of the I/O ports can be programed to special function via special control register. The detail functions are as follows:

- P2.0 to P2.3: Four 15mA sink current normal I/O pins only
- P3.0 to P3.3: Multi-function I/O pins (selected by P3IO register)
  - Normal function I/O pins
  - Special function I/O pins

P3IO register: (address = 00FH, default data = 0H)

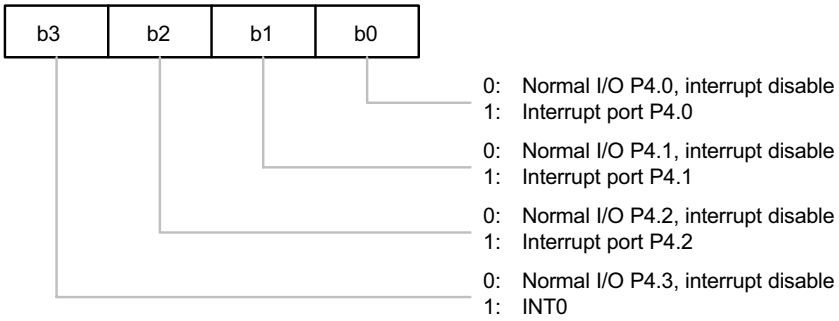


⌀ P4.0 to P4.3: Multi-function I/O pins (selected by P4IO register)

– Normal function I/O pins

– Special function I/O pins

P4IO register: (address = 010H, default data = 0H)

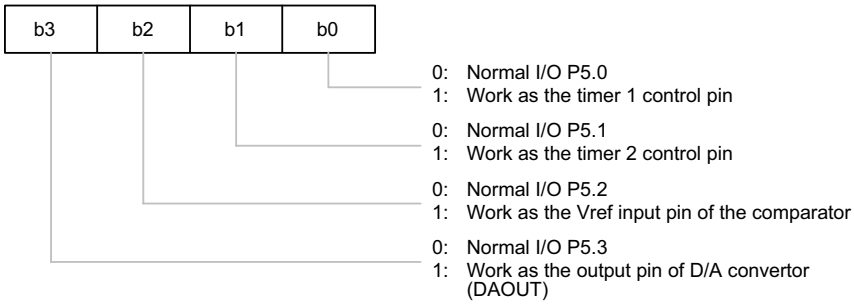


⌀ P5.0 to P5.3: Multi-function I/O pins (selected by P5IO register)

– Normal function I/O pins

– Special function I/O pins

P5IO register: (address = 011H, default data = 0H)

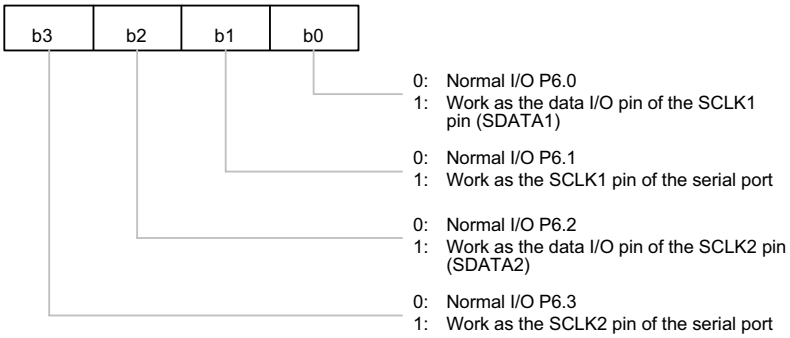


⌀ P6.0 to P6.3: Multi-function I/O pins (selected by P6IO register)

– Normal function I/O pins

– Special function I/O pins

P6IO register: (address = 012H, default data = 0H)



⌀ PA.0 to PA.3: Normal function I/O pins only

⌀ PB.0 to PB.3: Normal function I/O pins only

⌀ PC.1 to PC.3: Normal function I/O pins only

⌀ PD.0 to PD.1: Normal function I/O pins only

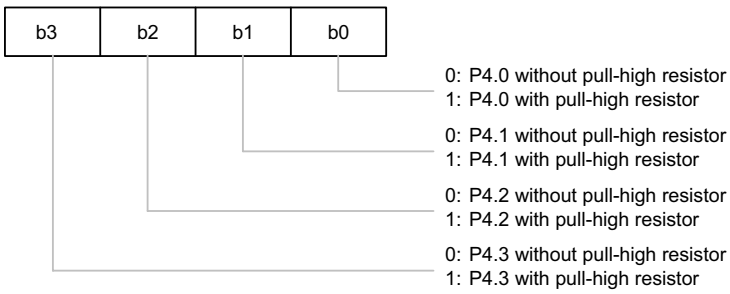
6.5.2 Pull High and Open Drain Control of I/O

Some of the above I/O ports can be controlled with pull-high resistor or open drain by programming the special register.

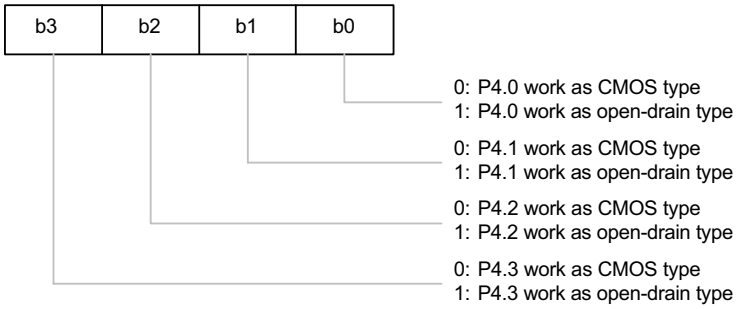
All pull-high resistors of the following descriptions are 100KΩ under 3.0 voltage test condition. After power-on reset the following special register will all reset to 0H.

⌀ P4.0 to P4.3:

H register: (address = 003H, default data = 0H)

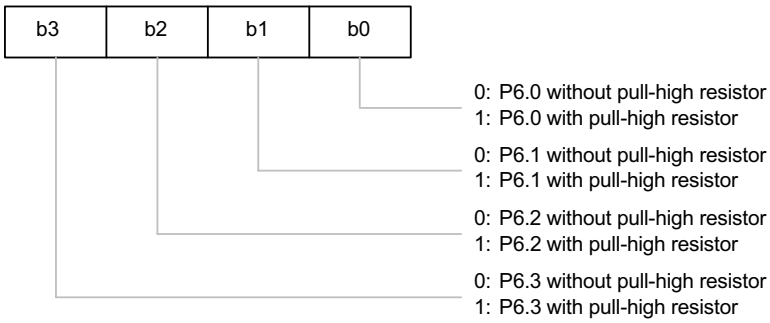


P4TP register: (address = 004H, default data = 0H)

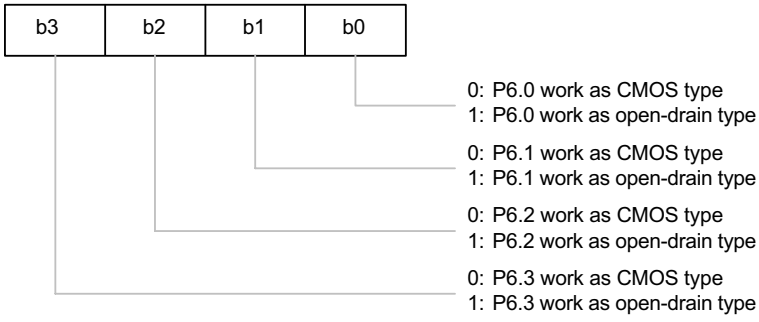


⌀ P6.0 to P6.3 :

P6PH register: (address = 005H, default data = 0H)

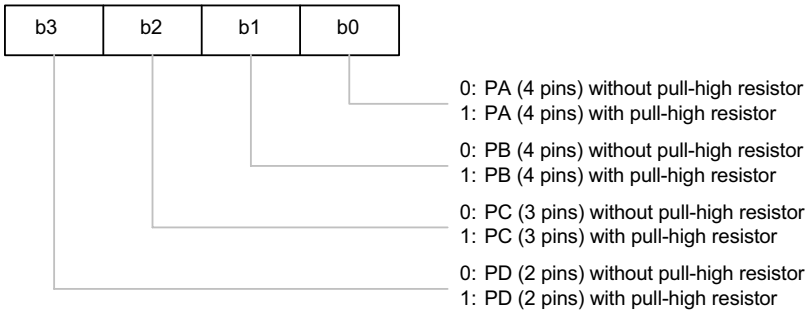


P6TP register: (address = 006H, default data = 0H)

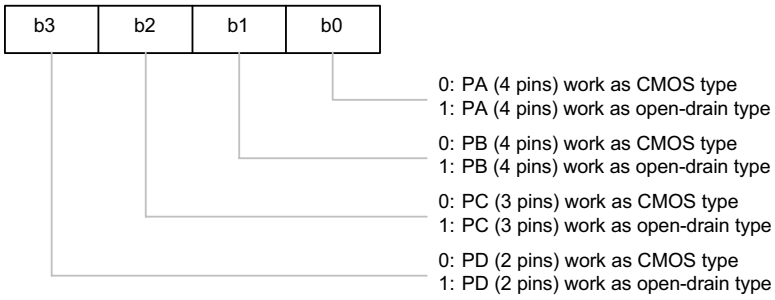


⌀ PA, PB, PC, PD:

PABCDPH register: (address = 007H, default data = 0H)

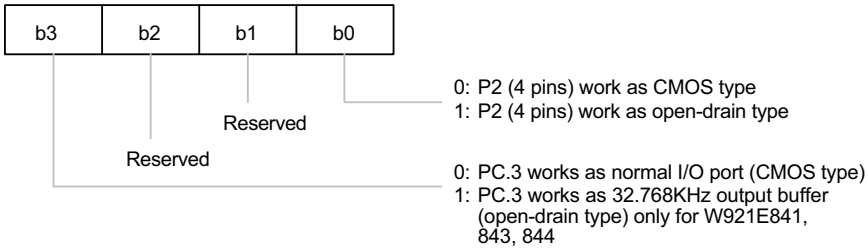


PABCDTP register: (address = 008H, default data = 0H)



⌀ P2:

P2TP register: (address = 00DH, default data = 0H)



6.6 Serial Port

The W921E840 has a clock-synchronous serial interface which transmits and receives 8-bit data as default. User can program the P6IO register to select port P6 as the serial port. The serial transmitter/receiver function can be operated with multi-nibble function and the LSB of every nibble is transmitted/received first.

The serial transmitted/received data are come from or are stored into the serial buffer registers (address 050H to 14EH); how many nibbles will be transmitted/received is decided by the serial MSB nibble register (SRMNR, address = 00AH) and serial LSB nibble register (SRLNR, address = 009H).

SRMNR register: (address = 00AH, default data = 0H)

b3	b2	b1	b0

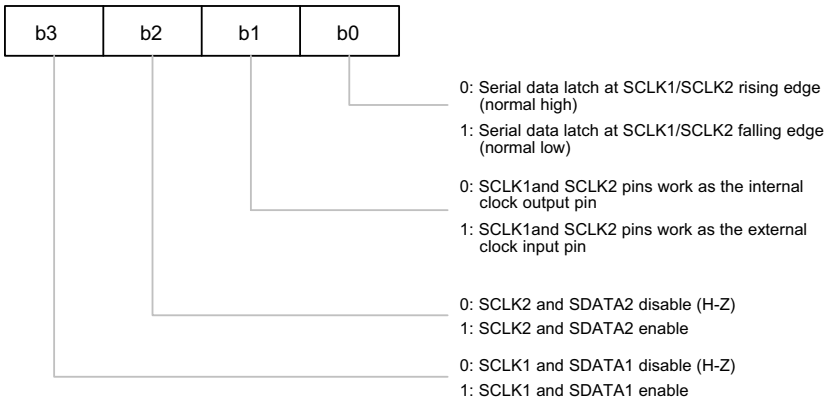
SRLNR register: (address = 009H, default data = 2H)

b3	b2	b1	b0

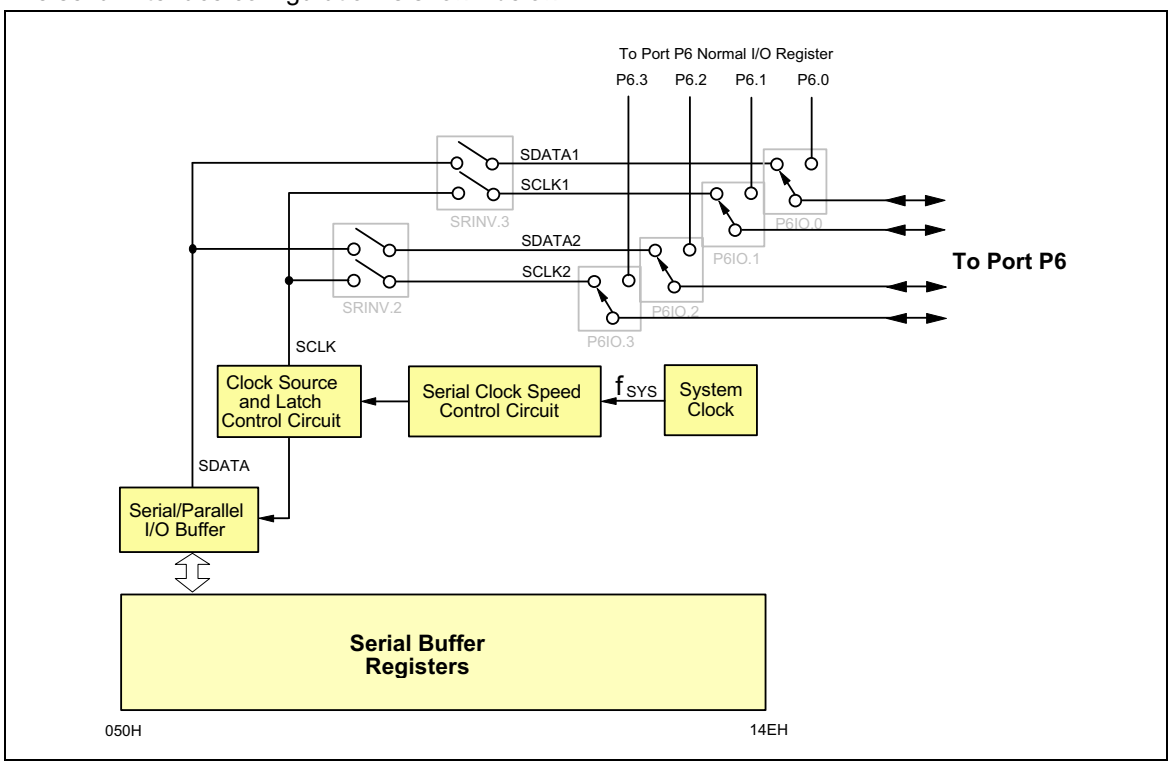
The default data in SRMNR and SRLNR are 0 and 2, meaning that the default serial interface is used to transmit/receive 8-bit data serially. As soon as the above two register are programmed and the instructions such as SOP or SIP are executed, the serial transmitter/receiver multi-nibble function will be performed. The transmitted/received number will be auto increased by one when each nibble is transmitted/received until the number is equal to SRLNR, SRMNR registers. Even if the HOLD instruction is executed, the SOP or SIP function will continue executing until the transmitter/receiver function has been completed. However, executing the STOP instruction will stop all serial transmitter/receiver function.

The transceiver data will be latched on the rising or falling edge of the clock; this is determined by the serial clock inverter control register (SRINV, address = 00CH). Before SOP or SIP instruction is executed the SRINV register must be set to the exact value. Once the bit3 and bit2 of SRINV register are both cleared to zero, the serial transceiver function will be reset to initial status immediately.

SRINV register: (address = 00CH, default data = 0H)

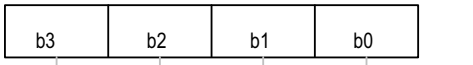


The serial interface configuration is shown below:



The internal serial clock can be controlled by the serial clock speed control register (SRSPC); the format is as follows:

SRSPC register: (address = 00BH, default data = 0H)



b3	b2	b1	b0	Input frequency
0	0	0	0	Reserved
0	0	0	1	fsys/4 Hz
0	0	1	0	fsys/8 Hz
0	0	1	1	fsys/16 Hz
0	1	0	0	fsys/32 Hz
0	1	0	1	fsys/64 Hz
0	1	1	0	fsys/128 Hz
0	1	1	1	fsys/256 Hz
1	0	0	0	fsys/512 Hz
1	0	0	1	fsys/1024 Hz
1	0	1	0	fsys/2048 Hz

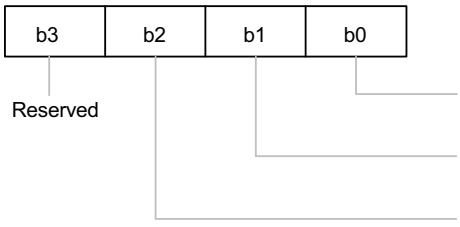
Normally the SCLK1 or SCLK2 pin will remain in high state and the serial data will be latched at the rising edge of the SCLK1 or SCLK2 signal, but the serial clock inverter control register (SRINV) will invert the above function. In this case SCLK1 or SCLK2 pin will remain in low state and the serial data will be latched at the falling edge of the SCLK1 or SCLK2 signal.

The transmitting serial clock can come from SCLK1 or SCLK2, depending on which one is enable. If the serial function is disabled, it will cause the relative pins to be high impendance and it will not affect the contents of serial buffer registers (start at address 050H).

6.7 DTMF Generator

There is one dual tone multi-frequency (DTMF) generator channel in this chip. The correct DTMF output frequency is decided by the OSCCTR register as shown below:

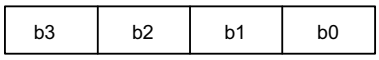
OSCCTR register: (address = 013H, default data = 0H)



b2	b1	b0	Osc. Selection
0	0	0	400 KHz
0	0	1	800 KHz
0	1	0	2 MHz
0	1	1	4 MHz
1	0	0	Reserved
1	0	1	3.58MHz

There are four bits in the DTMF register; the functions are described in the following table:

DTMF register: (address = 014H, default data = 0H)

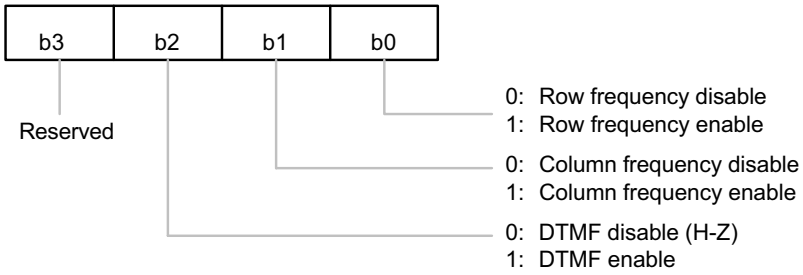


b3	b2	b1	b0	Function Description
X	X	0	0	Column 1 (1209 Hz) output
X	X	0	1	Column 2 (1336 Hz) output
X	X	1	0	Column 3 (1477 Hz) output
X	X	1	1	Column 4 (1633 Hz) output
0	0	X	X	Row 1 (697 Hz) output
0	1	X	X	Row 2 (770 Hz) output
1	0	X	X	Row 3 (852 Hz) output
1	1	X	X	Row 4 (941 Hz) output

Note: X ~ don't care

The output frequency of the row and column will be controlled by the row/column frequency control register (RCCTL).

RCCTL register: (address = 015H, default data = 0H)



The following table shows the DTMF keypad and its frequency.

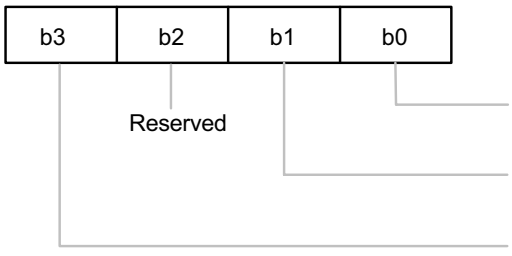
C1	C2	C3	C4	
1	*2*	*3*	*A*	R1
4	*5*	*6*	*B*	R2
7	*8*	*9*	*C*	R3
*	*0*	#	*D*	R4

Key	Frequency
R1	697 Hz
R2	770 Hz
R3	852 Hz
R4	941 Hz
C1	1209 Hz
C2	1336 Hz
C3	1477 Hz
C4	1633 Hz

6.8 Beep Tone Generator

There are four kinds of frequency that can output from the BTG pin that works as beep tone generator. The BTG pin can output the special frequency—2 KHz, 1 KHz, 630 Hz or 520 Hz, and the correct output frequency is decided by the OSCCTR register (address = 013H) and BTGR register (address = 03FH) as shown below:

BTGR register: (address = 03FH, default data = 0H)



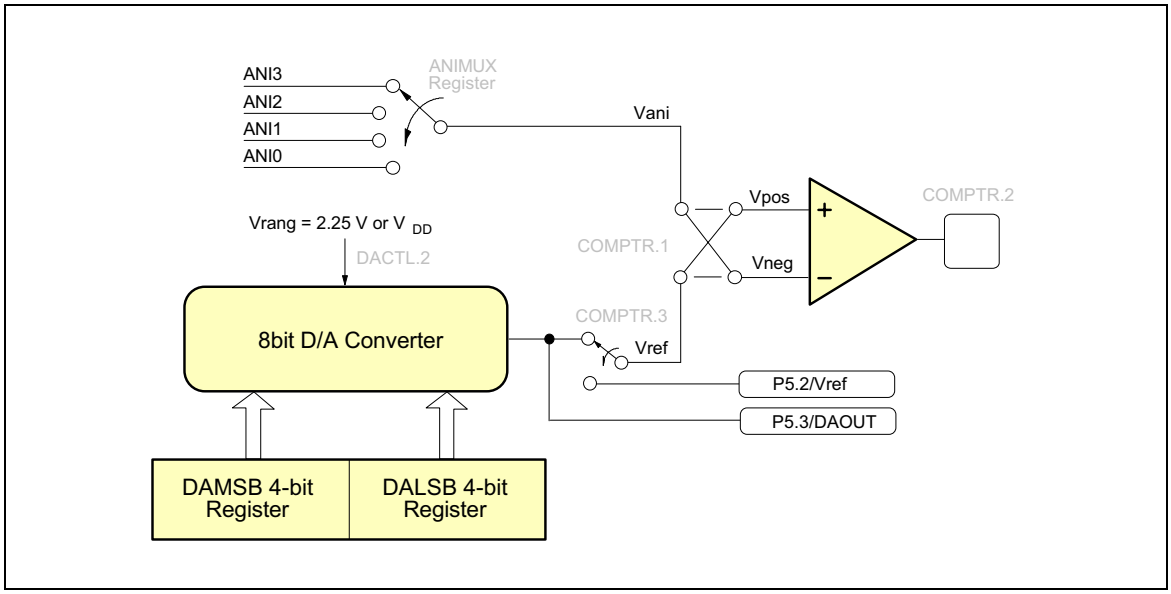
b1	b0	Output Freq.
0	0	2K Hz
0	1	1K Hz
1	0	630 Hz
1	1	520 Hz

0: Disable beep tone generator
(BTG pin keep in high state)
1: Enable beep tone generator

If the beep tone generator is disabled by setting bit 3 of the BTGR register to zero or after power on reset, the BTG output pin will remain in high state.

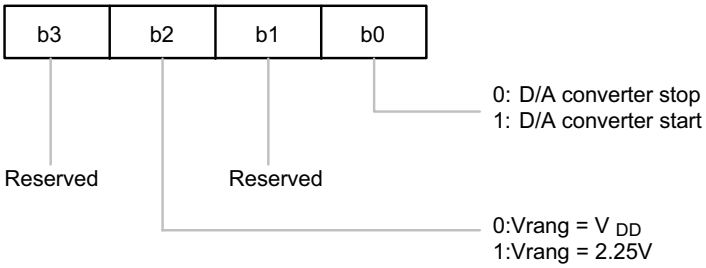
6.9 D/A Converter

The content of 8-bit D/A converter is divided into D/A MSB data register (DAMSB) and D/A LSB data register (DALSB). The block diagram is shown below.



⌀ D/A Converter Control Register:

DACTL register: (address = 016H, default data = 0H)



When the DACTL register bit0 is set by software, the 8-bit D/A converter starts converting. The only way to disable the D/A converter is to reset the bit0 of the DACTL register using the software control. The analog signal will be output to the P5.3 pin in this chip if the I/O port works as the D/A output pin.

The power source of the D/A converter (R-2R circuit) can be selected from the V_{DD} or 2.25V by programming the DACTL register bit2.

⌀ D/A Converter LSB Data Register

DALSB register: (address = 017H, default data = 0H)

b3	b2	b1	b0

⌀ D/A Converter MSB Data Register

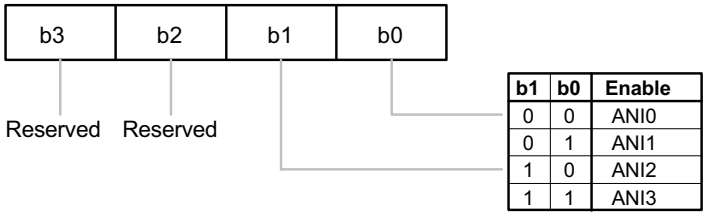
DAMSB register: (address = 018H, default data = 0H)

b3	b2	b1	b0

6.10 Comparator

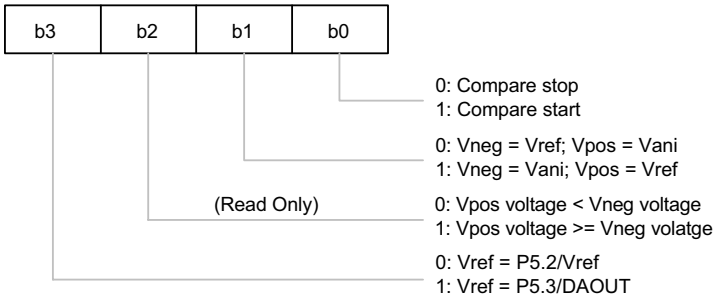
There are 4-channel inputs to the comparator negative (can be programmed to positive) terminal, but only one channel will be active at a time. The control register is shown below.

ANIMUX register: (address = 019H, default data = 0H)



b1	b0	Enable
0	0	ANI0
0	1	ANI1
1	0	ANI2
1	1	ANI3

COMPTR register: (address = 01AH, default data = 4H)



When the COMPTR register bit0 is set by software, the comparator starts and the bit2 of the COMPTR register will be set to "1" initially. The comparing result will be stored in the bit2 of the COMPTR register and will keep this value until the bit0 of the COMPTR register is set again. The only way to disable the comparator is to reset the bit0 of the COMPTR register using the software control.

The initial value of the COMPTR bit2 is "1", the falling edge of COMPTR bit2 will cause the comparator interrupt to become active if the enable flag of the comparator interrupt is set.

The bit3 of the COMPTR register controls the source of Input voltage reference (Vref). The input reference voltage (Vref) comes from external pin (P5.2/Vref) or D/A converter analog signal output (P5.3/DAOUT).

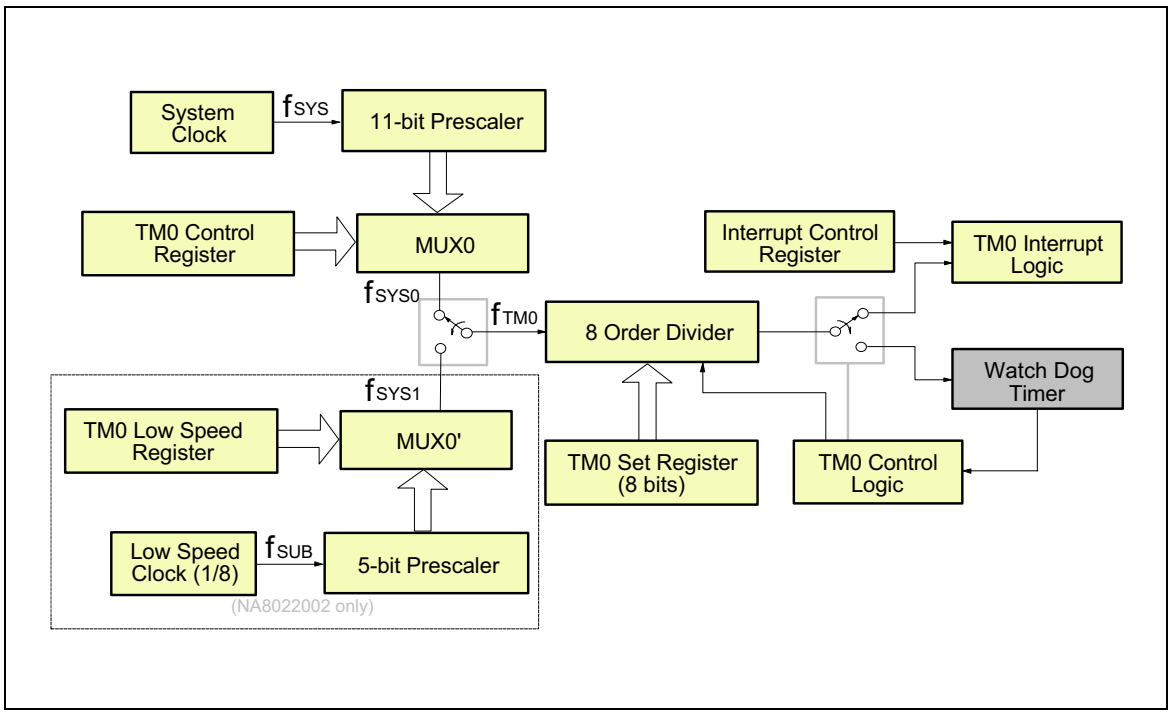
6.11 Timer/Counter

There are four timers (TM0, TM1, TM2 and TM3) in this chip, and all can be initialized at any time by writing data into the TM0, TM1, TM2 and TM3 set register.

6.11.1 TM0

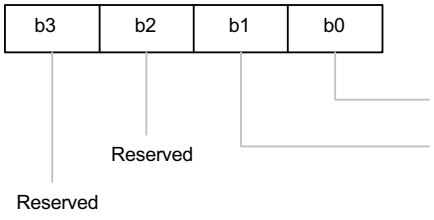
TM0 can perform the following functions:

1. 2 to19 order divider
2. Auto-reload timer
3. Watch-dog timer



The format of the TM0 control register (TM0CR) is described below:

TM0CR register: (address = 020H, default data = 0H)



b1	b0	Input frequency (f_{SYS0})
0	0	fsys/2 Hz
0	1	fsys/256 Hz
1	0	fsys/1024 Hz
1	1	fsys/2048 Hz

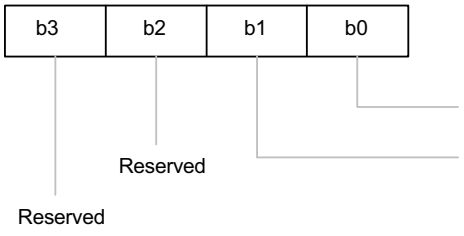
The TM0 set register is divided into TM0 MSB data register (TM0MSB register, address = 021H, default = 0FH) and TM0 LSB data register (TM0LSB register, address = 022H, default = 0FH).

TM0 will overflow when TM0 set register is from 00H to 0FFH and the value in the TM0MSB and TM0LSB will be auto reloaded to the TM0 set register when the STTM0 bit2 is set. TM0 will decrease by 1 at the frequency of timer 0 clock after timer 0 has started.

If at any time the STTM0 bit3 is from 0 to 1 (disable to enable) in the timer mode, the TM0MSB and TM0LSB will be auto reloaded to the TM0 set register again and restart the timer 0. TM0 will stop operating while the STTM0 bit3 is reset to 0.

The format of the TM0 low speed register (TM0LSR) is described below:

TM0LSR register: (address = 024H, default data = 0H, only for W921E841, 843, 844)



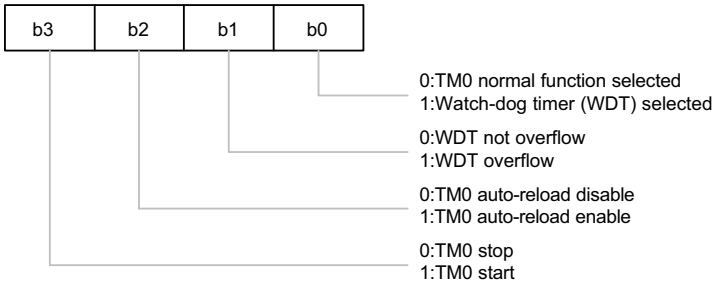
b1	b0	Input frequency (f_{SYS1})
0	0	fsys/2 Hz
0	1	fsys/256 Hz
1	0	fsys/1024 Hz
1	1	fsys/2048 Hz

The TM0 starts to down count when the STTM0 register bit3 is set. When TM0 overflows, the STTM0 bit3 will be reset by hardware to stop TM0 if the auto-reload is disabled, but the STTM0 bit3 will not be reset if the auto-reload is enabled.

When the TM0 normal function is performed, the watch-dog timer function will be disabled automatically.

The format of the TM0 status register (STTM0) is described below:

STTM0 register: (address = 023H, default data = 0H)



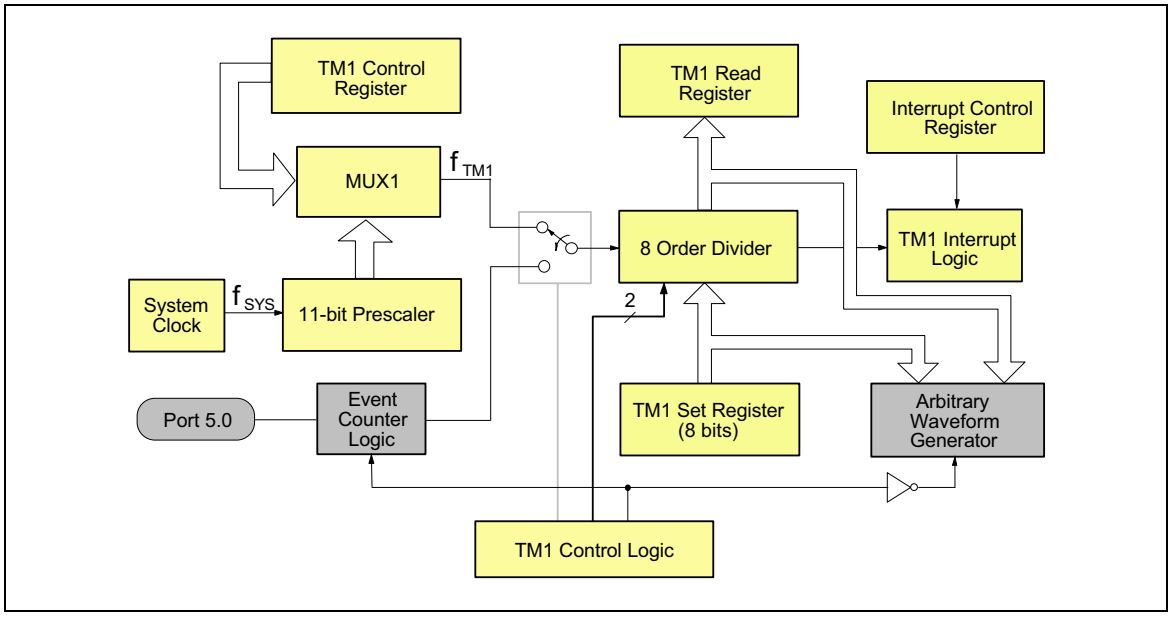
If TM0 works as the watch-dog timer (WDT), the bit1 of the STTM0 register will be set when the WDT is overflow, in the meanwhile, the system is reset just as with power on reset except the STTM0 bit1. The WDT (STTM0 bit1) will be reset to zero only with the power on reset or the RAM write mode.

In the timer mode or event counter mode the time out will be the programming data add 1 ([TM0MSB, TM0LSB]+1). It is the same in the TM1, TM2 and TM3.

6.11.2 TM1

TM1 can perform the following functions:

1. 2 to19 order divider
2. Auto-reload timer
3. Arbitrary waveform generator
4. Event counter



The format of the TM1 control register (TM1CR) is described below:

TM1CR register: (address = 025H, default data = 0H)

b3	b2	b1	b0

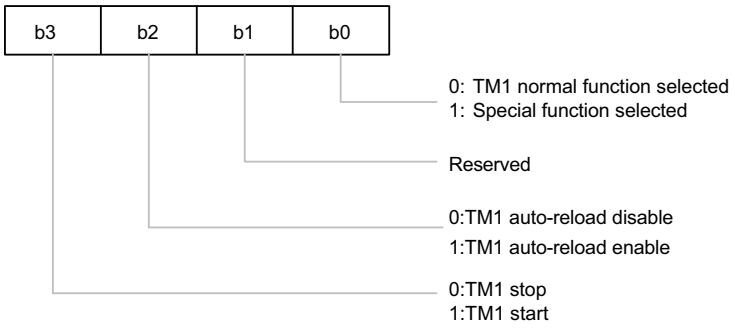
b3	b2	b1	b0	Input frequency (f_{TM1})
0	0	0	0	fsys/2 Hz
0	0	0	1	fsys/4 Hz
0	0	1	0	fsys/8 Hz
0	0	1	1	fsys/16 Hz
0	1	0	0	fsys/32 Hz
0	1	0	1	fsys/64 Hz
0	1	1	0	fsys/128 Hz
0	1	1	1	fsys/256 Hz
1	0	0	0	fsys/512 Hz
1	0	0	1	fsys/1024 Hz
1	0	1	0	fsys/2048 Hz

The TM1 set register is divided into TM1 MSB data register (TM1MSB register, address = 026H, default = 0FH) and TM1 LSB data register (TM1LSB register, address = 027H, default = 0FH).

The TM1 read register is divided into TM1 read only MSB data register (TM1RM register, address = 01CH, default = 0FH) and TM1 read only LSB data register (TM1RL register, address = 01DH, default = 0FH).

The format of the TM1 status register (STTM1) is described below:

STTM1 register: (address = 028H, default data = 0H)



If the TM1 is in the timer mode, divider will overflow when it is from 00H to 0FFH and the value in the TM1MSB and TM1LSB will be auto reloaded into the TM1 set register when the STTM1 bit2 is set. TM1 will decrease by 1 at the frequency of timer 1 clock after timer 1 has started.

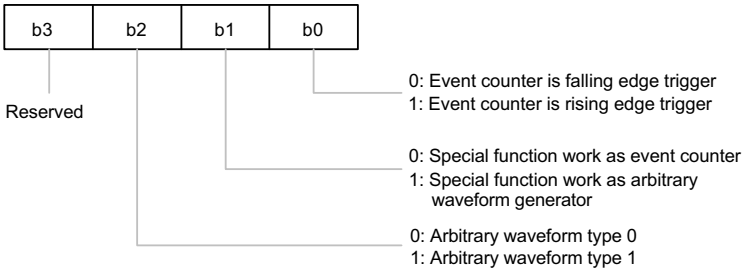
At any time the STTM1 bit3 is from 0 to 1 (disable to enable) the TM1MSB and TM1LSB will be auto reloaded to the TM1 set register again and restart the TM1. TM1 will stop operating while the STTM1 bit3 is reset to 0.

The TM1 starts to down count when the STTM1 register bit3 is set. When TM1 overflows, the STTM0 bit3 will be reset by hardware to stop TM1 if the auto-reload is disabled, but the STTM1 bit3 will not be reset if the auto-reload is enable.

When the TM1 normal timer function is performed, the special function (event counter or arbitrary waveform generator) will be disabled automatically. The special function input or output is from or to P5.0 and the debounce time is one system clock (f_{SYS}).

The format of the TM1 trigger/event counter condition register (TGTM1) is described below:

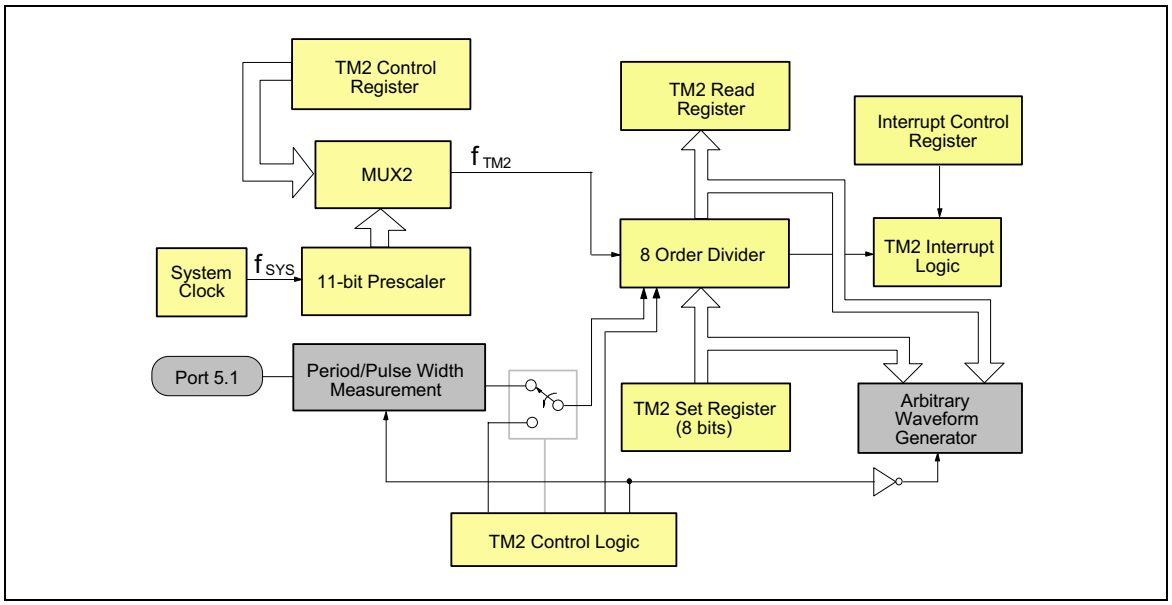
TGTM1 register: (address = 029H, default data = 0H)



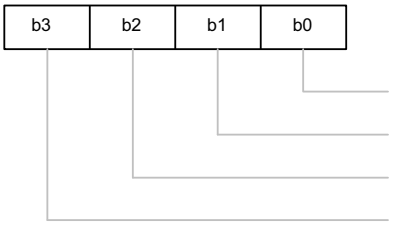
6.11.3 TM2

TM2 can perform the following functions:

1. 2 to19 order divider
2. Auto-reload timer
3. Arbitrary waveform generator
4. Period/pulse width measurement function



TM2CR register: (address = 02AH, default data = 0H)



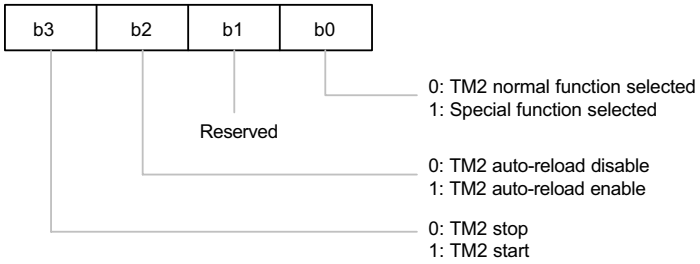
b3	b2	b1	b0	Input frequency (f_{TM2})
0	0	0	0	fsys/2 Hz
0	0	0	1	fsys/4 Hz
0	0	1	0	fsys/8 Hz
0	0	1	1	fsys/16 Hz
0	1	0	0	fsys/32 Hz
0	1	0	1	fsys/64 Hz
0	1	1	0	fsys/128 Hz
0	1	1	1	fsys/256 Hz
1	0	0	0	fsys/512 Hz
1	0	0	1	fsys/1024 Hz
1	0	1	0	fsys/2048 Hz

The TM2 set register is divided into TM2 MSB data register (TM2MSB register, address = 02BH, default = 0FH) and TM2 LSB data register (TM2LSB register, address = 02CH, default = 0FH).

The TM2 read register is divided into TM2 read only MSB data register (TM2RM register, address = 01EH, default = 0FH) and TM2 read only LSB data register (TM2RL register, address = 01FH, default = 0FH).

The format of the status of TM2 register (STTM2) is described below:

STTM2 register: (address = 02DH, default data = 0H)



If the TM2 is in the timer mode, divider will overflow when it is from 00H to 0FFH and the value in the TM2MSB and TM2LSB will be auto reloaded to the TM2 set register. TM2 will decrease by 1 at the frequency of timer 2 clock after timer 2 has started.

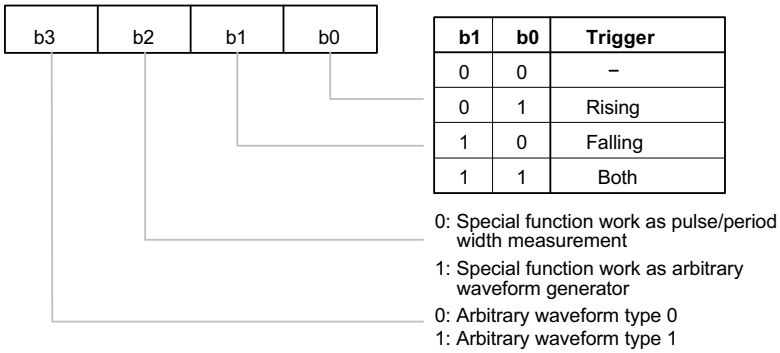
If at any time the STTM2 bit3 is from 0 to 1 (disable to enable) the TM2MSB and TM2LSB will be auto reloaded to the TM2 set register again and restart the TM2. TM2 will stop operating when the STTM2 bit3 is reset to 0

The TM2 starts to count when the STTM2 register bit3 is set. When TM2 overflows, the STTM0 bit3 will be reset by hardware to stop TM2 if the auto-reload is disabled, but the STTM2 bit3 will not be reset if the auto-reload is enabled.

When the TM2 normal function is performed, the special function will be disabled automatically.

The format of the TM2 trigger condition register (TGTM2) is shown below:

TGTM2 register: (address = 02EH, default data = 0H)



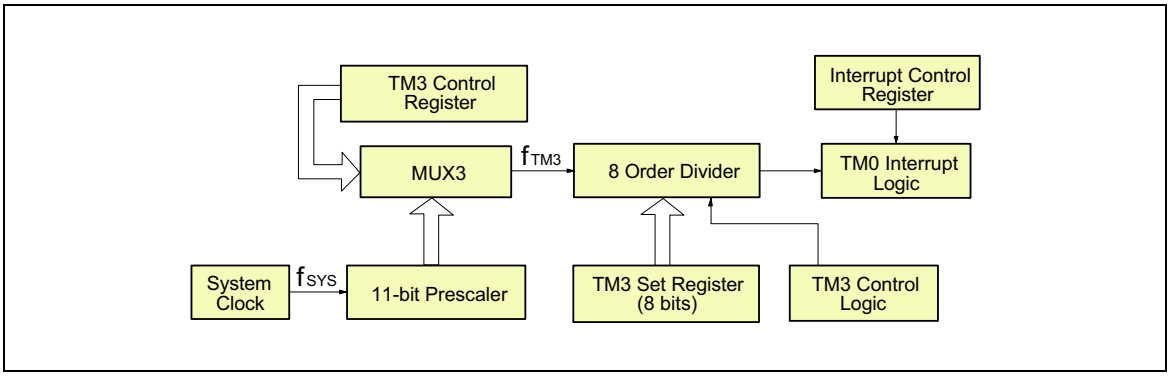
b1	b0	Trigger
0	0	–
0	1	Rising
1	0	Falling
1	1	Both

In the pulse/period width measurement mode the measuring-data is the 1'S complement of the exact data and the TM2 interrupt flag is set every 255 timer clock past or the 2nd trigger condition occurs. So the measured pulse/period width is $(255(N-1)+\overline{TM2})*T$, *N* is the number of interrupt flag occurs, $\overline{TM2}$ is the 1'S complement of timer2 register, *T* is the period of timer 2 clock. The special function input or output is from or to P5.1.

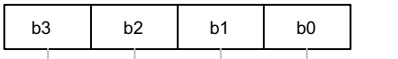
6.11.4 TM3

TM3 can perform the following functions:

1. 2 to19 order divider
2. Auto-reload timer



TM3CR register: (address = 02FH, default data = 0H)

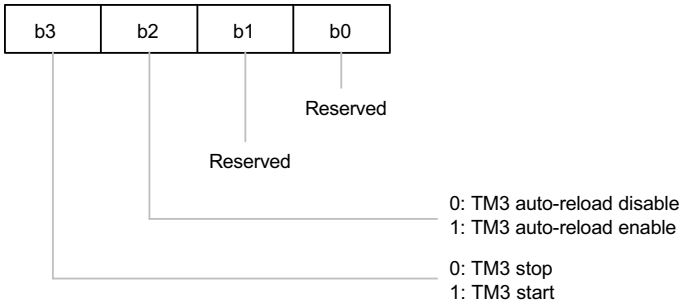


b3	b2	b1	b0	Input frequency (f_{TM3})
0	0	0	0	fsys/2 Hz
0	0	0	1	fsys/4 Hz
0	0	1	0	fsys/8 Hz
0	0	1	1	fsys/16 Hz
0	1	0	0	fsys/32 Hz
0	1	0	1	fsys/64 Hz
0	1	1	0	fsys/128 Hz
0	1	1	1	fsys/256 Hz
1	0	0	0	fsys/512 Hz
1	0	0	1	fsys/1024 Hz
1	0	1	0	fsys/2048 Hz

The TM3 set register is divided into TM3 MSB data register (TM3MSB register, address = 030H, default = 0FH) and TM3 LSB data register (TM3LSB register, address = 031H, default = 0FH).

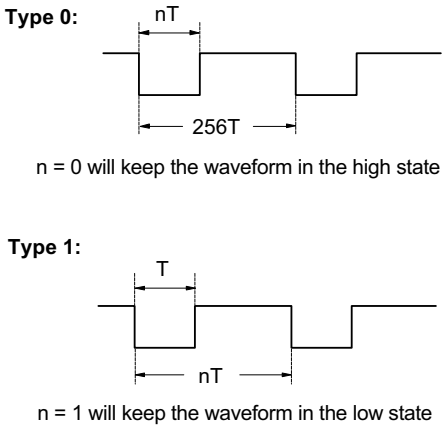
The format of the status of TM3 register (STTM3) is described below:

STTM3 register: (address = 032H, default data = 0H)



6.11.5 Arbitrary Waveform Generator

The TM1 and TM2 have the arbitrary waveform generator circuit. Both have the same function as the following description.



Note: n is the value stored in the TM1 set register or TM2 set register

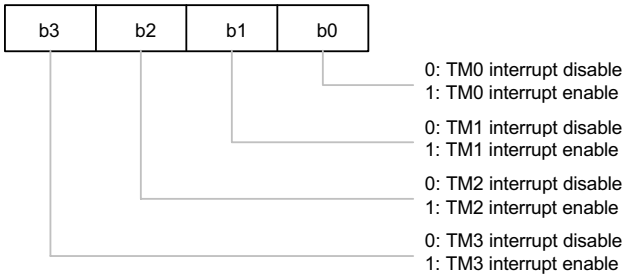
6.12 Interrupt

There are eight interrupt sources (two external and six internal sources) in the W921E840. All the pins of external sources~INT0 (P4.3) and port P4 (P4.0 to P4.2)~are falling edge active.

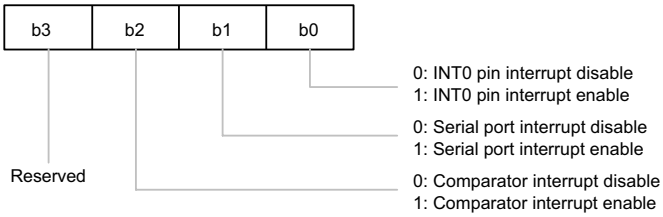
6.12.1 Interrupt Control Register

Which interrupt is enabled is controlled by the interrupt control register1 to 3 (INTCT1 to INTCT3). The formats are shown below:

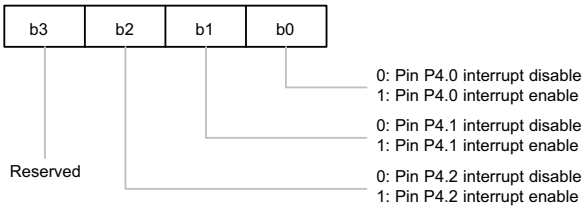
INTCT1 register: (address = 039H, default data = 0H)



INTCT2 register: (address = 03AH, default data = 0H)



INTCT3 register: (address = 03BH, default data = 0H)

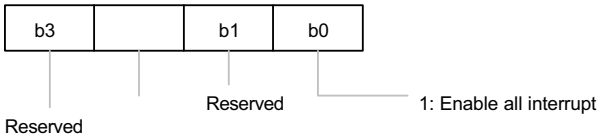


6.12.2 Interrupt Enable Flag

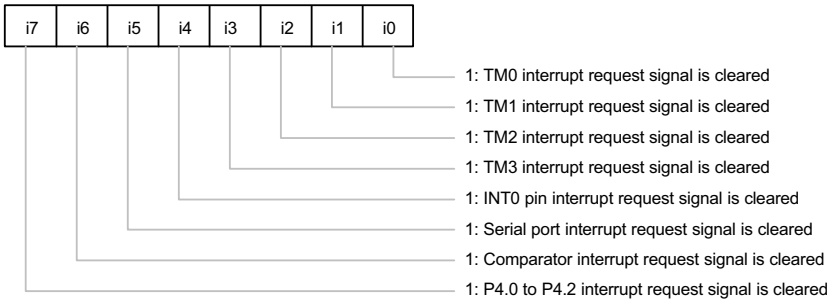
When the interrupt is enabled by the event, the program counter will jump to the interrupt address and the enable interrupt flag (ENINT) bit0 is cleared, at the same time, all the interrupt will be disabled.

The only way to enable the interrupt again is to set the ENINT bit0 or execute the RTNI instruction.

ENINT register: (address = 034H, default data = 0H)



When the interrupt is enabled by the event, the individual interrupt request signal is cleared by the hardware automatically, but the other interrupt request signals will remain the same condition. The only method of resetting the interrupt request signal is to execute the instruction CLR EVF, #I, it is a 2 words / 2 cycles instruction; the format of the immediate data is shown below.



6.13 Operating Mode

There are three types of operating mode in this chip — normal mode, hold mode and stop mode.

6.13.1 Normal Mode

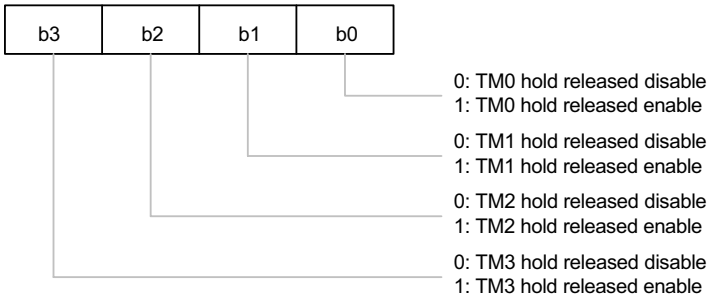
All functions works well and the μC operates according to the clock generated by the system clock.

6.13.2 Hold Mode

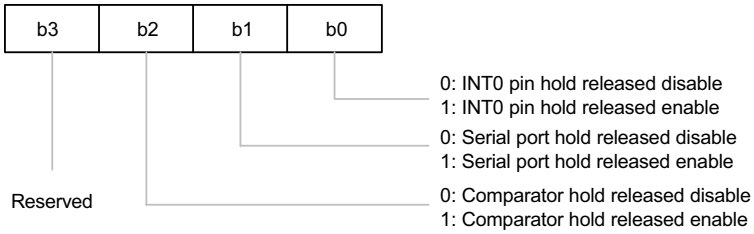
In hold mode, all operations of μC cease, except for the operation of the oscillator, timer/counter, serial port and interrupt active pins. The μC enters hold mode when the HOLD instruction is executed.

The hold mode can be released only by the $\overline{\text{RESET}}$ pin or the interrupt request signal. Before The device enters the hold mode, the hold mode release flag1, 2, 3 (HMRF1, 2, 3, address = 036H, 037H, 038H) must be set to define the hold mode release conditions. If interrupt condition is met and enabled in hold mode, the interrupt will be accepted to release hold mode and jump to interrupt vector to execute interrupt service routine. For more details, refer to the following flags and flow chart.

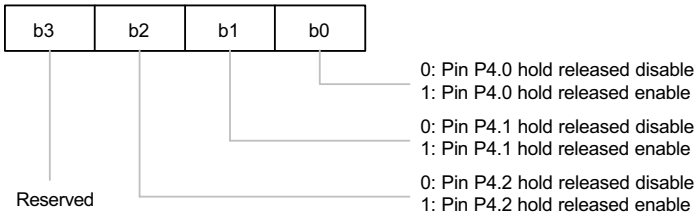
HMRF1 register: (address = 036H, default data = 0H)



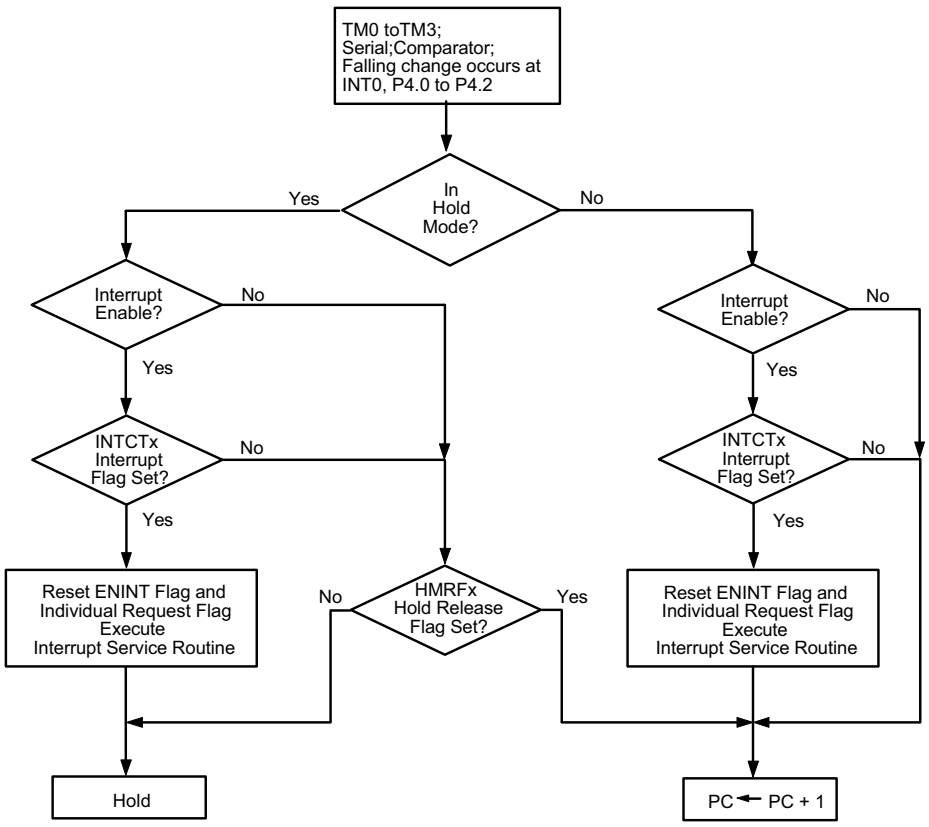
HMRF2 register: (address = 037H, default data = 0H)



HMRF3 register: (address = 038H, default data = 0H)



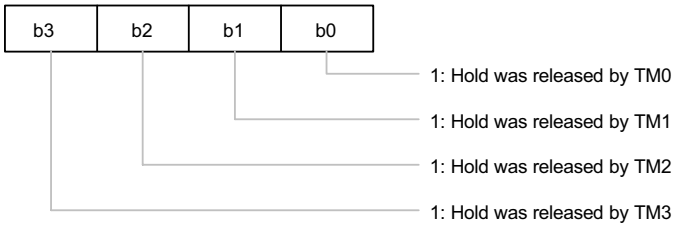
Hold mode operation flow chart



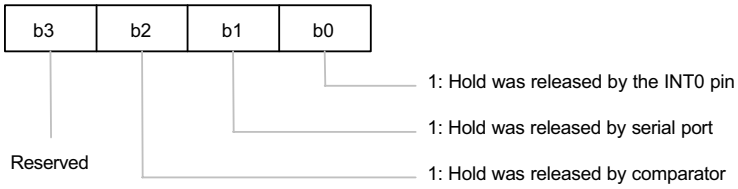
note: x is the corresponding flag bit of interrupt enable or hold mode release register

The hold released status flag1, 2, 3 (HRSTS1, 2, 3, address = 03CH, 03DH, 03EH) indicate by which interrupt source the hold mode has been released, and is loaded by hardware. When any bit of HRSTS1, 2, 3 is "1," the hold mode will be released and HOLD instruction in invalid. The bit descriptions are as follows:

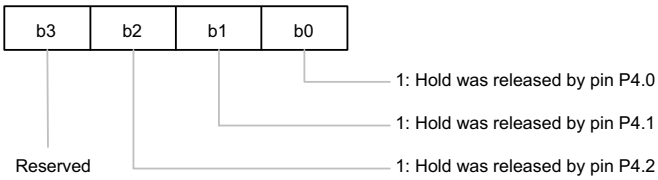
HRSTS1 register: (address = 03CH, read only, default data = 0H)



HRSTS2 register: (address = 03DH, read only, default data = 0H)



HRSTS3 register: (address = 03EH, read only, default data = 0H)



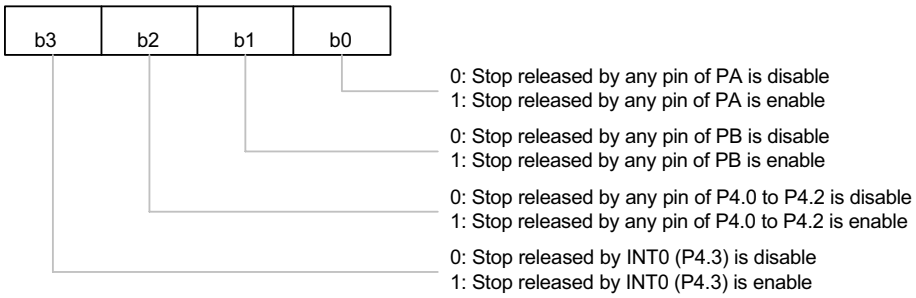
HRSTS1, 2 and 3 are read only registers and can be reset by the instruction CLR EVF, #I. When EVF has been reset, the corresponding bit of HRSTSn (n = 1 to 3) is reset simultaneously.

6.13.3 Stop Mode

The μC enters the stop mode only when the STOP instruction is executed. Because the oscillator is stopped, all functions in this chip are stopped.

The stop mode can be released by the $\overline{\text{RESET}}$ pin, INT0 pin, P4.0 to P4.2, PA port or PB port. The stop condition release flag (STPRF, address = 035H) is the stop mode release control register.

STPRF register: (address = 035H, default data = 8H)



When stop mode is active, if the stop condition release flag (STPRF) is set before the STOP instruction is executed, the low level signal on the P4, PA or PB ports will release the stop mode and a delay of 256 machine cycles occurs right after the stop mode is released, then the next instruction is executed or the program counter (PC) jumps to interrupt subroutine if the interrupt is enabled and interrupt request exists.

The control flow chart is shown below:

Stop mode operation flow chart